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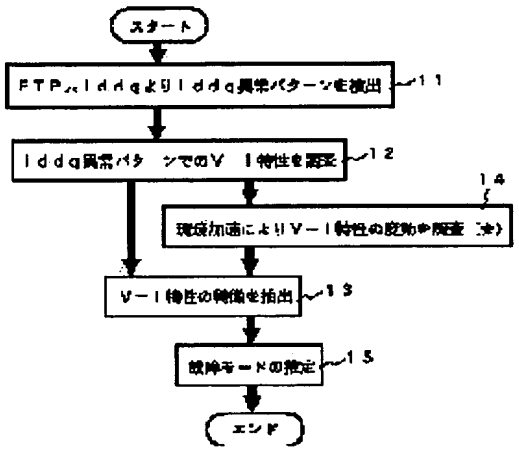
(54) SPECIFYING METHOD FOR FAILURE MODE

(57)Abstract:
PURPOSE: To provide a specifying method for a failure mode, capable of specifying the failure mode in nondestruction easily and speedily.
CONSTITUTION: When a logical motion test pattern (FTP) is inputted to a CMOS logical circuit, a leak current Iddq in a static state of logical motion extracts this FTP at a time when abnormality of this leak current Iddq flowing beyond a specified value is produced. A relationship of supply voltage vs. supply current known called a 'V-I characteristic' in the FTP at the time when this Iddq abnormality is produced, is examined. Next, the distinctive feature of this examined V-I characteristic curve is extracted. When a failure mode is not narrowed down at stationary environment, the power source impression of a large scale integrated circuit LSI is contrived or the physical environment of this LSI to be measured in varied to some extent, and by emphasizing the feature of this V-I characteristic curve, the failure mode is clearly actualized. Then, the failure mode is specified on the basis of the examined V-I characteristic.



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CLAIMS

[Claim(s)]
[Claim 1] The logic actuation test pattern of arbitration is inputted one by one from the input terminal of a CMOS logical circuit. The power-source current in the quiescent state of logic actuation of this CMOS logical circuit is measured, respectively. Among those, the logic actuation test pattern which the abnormalities to which the power-source current in the quiescent state of logic actuation flows exceeding a predetermined value generate is extracted. The specific approach of the failure mode characterized by specifying failure mode from the change property curve of a power-source current which changes according to change of supply voltage where the extracted this logic actuation test pattern is impressed.
[Claim 2] The change property curve of a power-source current which changes according to change of supply voltage where said extracted logic actuation test pattern is impressed is the specific approach of the failure mode according to claim 1 which carries out the description of being the curve of a supply voltage pair power-source current characteristic which changes by changing the power-source impression environment of said CMOS logical circuit.
[Claim 3] Change of the power-source impression environment of said CMOS logical circuit is the specific approach of the failure mode according to claim 2 characterized by being change for every time amount of the arbitration of said supply voltage pair current characteristic where fixed supply voltage is impressed.
[Claim 4] Change of the power-source impression environment of said CMOS logical circuit is the specific approach of the failure mode according to claim 2 characterized by being change for every time amount of the arbitration of said supply voltage pair current characteristic where a fixed abnormality quiescent-state power-source current is passed.
[Claim 5] Change of the power-source impression environment of said CMOS logical circuit is the specific approach of the failure mode according to claim 2 characterized by being impressing a pulse voltage to supply voltage and changing said supply voltage pair current characteristic.
[Claim 6] Change of the power-source impression environment of said CMOS logical circuit is the specific approach of the failure mode according to claim 2 characterized by being making the polarity of the supply voltage to impress into reverse, and changing said supply voltage pair current characteristic.
[Claim 7] The change property curve of a power-source current which changes according to change of supply voltage where said extracted logic actuation test pattern is impressed is the specific approach of the failure mode according to claim 1 which carries out the description of being the curve of a supply voltage pair power-source current characteristic which changes by changing the physical environment of said CMOS logical circuit.
[Claim 8] Change of the physical environment of said CMOS logical circuit is the specific approach of the failure mode according to claim 7 characterized by being changing the outside temperature of a large-scale integrated circuit which has this CMOS logical circuit.
[Claim 9] Change of the physical environment of said CMOS logical circuit is the specific approach of the failure mode according to claim 7 characterized by being the existence of an exposure of the light on the front face of a chip of the large-scale integrated circuit which has this CMOS logical circuit.
[Claim 10] Change of the physical environment of said CMOS logical circuit is the specific approach of the failure mode according to claim 7 characterized by being the existence of an exposure of the ion on the front face of a chip of the large-scale integrated circuit which has this CMOS logical circuit.
[Claim 11] Change of the physical environment of said CMOS logical circuit is the specific approach of the failure mode according to claim 7 characterized by being the existence of an exposure of the electron on the front face of a chip of the large-scale integrated circuit which has this CMOS logical circuit.
[Claim 12] It is [claim 1 characterized by to detect failure mode, using respectively the inclination of the supply voltage value to which a power source current begins to flow rapidly in this supply voltage pair power source current characteristic, and a power source current, and the singular point of a property since failure mode specifies from the change property curve of a power source current which changes according to change of supply voltage where the logic actuation test pattern which said abnormalities generate is impressed thru/or] the specific approach of failure mode given in any 1 term among 11.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the specific approach of failure mode, and when especially a certain logic test pattern is inputted, it relates to the approach of specifying the failure mode generated in the CMOS logical circuit which the abnormalities in leakage current in the quiescent state of the logic called Iddq generate.
[0002]
[Description of the Prior Art] Conventionally, the method of specifying the cause of generating of the failure generated inside the CMOS logical circuit from electrical characteristics was impossible except for the short circuit between power sources (short circuit between Vdd-GND). Therefore, the failure generating part was narrowed down using the logic test pattern, physical analysis of the failure part narrowed down to the degree was performed, and the cause of fault is investigated and detected.
[0003] First, narrowing down of a failure part had the typical technique of extracting the potential map of an irradiating point, and a logic wave by detecting the secondary electron which is called an EB tester and which irradiates an electron on wiring of a large-scale integrated circuit (LSI), and is generated.
[0004] Moreover, detection of a failure part had detected failure mode using microscopes (SEM, optical microscope, etc.) by performing appearance observation, or etching to a desired layer with laser etc. further, and observing [**** / exposing a failure part] by performing ******** of the part limited by the ion beam which is called FIB, and which converged.
[0005] The method using the emission microscope (EMS) as a method which presumes failure mode is learned conventionally, and it is proposed by the 4th time dependability symposium (Vol.13/No.3 / November, 1991) "examination of the failure analysis technique of LSI by luminescence wavelength distribution" P.71 to P.76 of REAJ. This method is an analysis method which presumes the failure mode of LSI by analyzing the spectrum of the light emitted from the failure part of LSI in an emission microscope.
[0006] Drawing 18 is an explanatory view for the analysis of LSI by the above-mentioned emission microscope. In this drawing, luminescence emitted from the failure part of LSI42 is observed by the optical microscope 43 placed above LSI42 carried on the DUT board 41. Luminescence observed by this optical microscope 43 is amplified with the font amplifier tube 45 called an image intensifier through the filter 44 which makes only the light wave length band of the arbitration called a band pass filter penetrate, is picturized by CCD camera 46, and is sent to an image processing system 47. In order that an emission microscope may detect minute luminescence from LSI42, a luminescence observation path is set in a dark room 48. Moreover, the image which was processed by the image processing system 47 and obtained is displayed by the cathode-ray tube (CRT) 49.
[0007] By this conventional failure mode specification approach, by combining the function which integrates the quantity of light detected in the emission microscope, and the filter 44 which makes only the light wave length band of arbitration penetrate with a band pass filter, the amount of luminescence for every wavelength band is measured, and failure mode is presumed by observing the spectrum resulting from each failure mode.
[0008]
[Problem(s) to be Solved by the Invention] however, poor leak according [the failure mode from which the failure mode detected in an emission microscope is detected by the specific method of the conventional failure mode mentioned above in the band since the light wave length band of a band pass filter 44 is limited with 400 to 1000nm] to poor opening of the gate electrode on a CMOS logical circuit, and gate oxide destruction -- further -- high resistance -- it is the short circuit between wiring by the conductor etc., and the failure mode detected was limited.
[0009] Moreover, although the failure mode detected was plotted by the graph which took the amount of luminescence in an arbitration graduation scale to the Y-axis called "luminescence spectrum", and took wavelength to the X-axis, the luminescence spectrum of the failure mode mentioned above is [variation] and was not deterministic. For example, drawing 19 is luminescence spectrum which shows the relation of the amount of luminescence to each wavelength of poor opening (inside B of drawing) of gate oxide destruction (inside A of drawing), and a gate electrode. When the variation in the spectrum configuration is mostly considered for the same configuration, it becomes impossible for the amount of luminescence to each wavelength of poor opening of gate oxide destruction and a gate electrode to presume failure mode to accuracy so that drawing 19 may show.
[0010] Moreover, in order to have to perform failure analysis by the emission microscope from detection of a failure generating part first, it takes time amount great by specification (or presumption) of failure mode. Furthermore, the emission microscope had the fault of limiting the narrowing-down part of failure in order to make impossible detection of luminescence under wiring in LSI which has multilayer-interconnection structure. When leakage current was still larger, since the quantity of light became immense, it had a fault of it becoming impossible to use an emission microscope.
[0011] This invention was made in view of the above point, and aims at offering the specific approach of failure mode that failure mode can be easily specified by un-destroying by using the supply voltage pair power-source current characteristic in the test pattern which the abnormalities in leakage current in the quiescent state of the logic called Iddq generated.
[0012] Moreover, other objects of this invention are to offer the specific approach of failure mode that failure mode can

be specified promptly.
[0013]
[Means for Solving the Problem] This invention inputs the logic actuation test pattern of arbitration one by one from the input terminal of a CMOS logical circuit in order to attain the above-mentioned object. The power-source current in the quiescent state of logic actuation of a CMOS logical circuit is measured, respectively. Among those, the logic actuation test pattern which the abnormalities to which the power-source current in the quiescent state of logic actuation flows exceeding a predetermined value generate is extracted. Failure mode is specified from the change property curve of a power-source current which changes according to change of supply voltage where the extracted logic actuation test pattern is impressed.
[0014] Moreover, the change property curve of a power-source current which changes according to change of supply voltage where the logic actuation test pattern which this invention extracted is impressed carries out the description of being the curve of a supply voltage pair power-source current characteristic which changes by changing the power-source impression environment of a CMOS logical circuit.
[0015] Where fixed supply voltage is impressed, change of the power-source impression environment of the above-mentioned CMOS logical circuit here The change for every time amount of the arbitration of a supply voltage pair current characteristic, Where a fixed abnormality quiescent-state power-source current is passed, or the change for every time amount of the arbitration of a supply voltage pair current characteristic, Or it is characterized by being impressing a pulse voltage to supply voltage and changing a supply voltage pair current characteristic, or making the polarity of supply voltage to impress into reverse, and changing a supply voltage pair current characteristic.
[0016] Moreover, the change property curve of a power-source current which changes according to change of supply voltage where the logic actuation test pattern which this invention extracted is impressed carries out the description of being the curve of a supply voltage pair power-source current characteristic which changes by changing the physical environment of a CMOS logical circuit.
[0017] Here, change of the physical environment of a CMOS logical circuit is characterized by being the existence of an exposure of the light on changing the outside temperature of a large-scale integrated circuit which has a CMOS logical circuit, or the front face of a chip of the large-scale integrated circuit which has a CMOS logical circuit, ion, or an electron.
[0018] Furthermore, in this invention, since failure mode is specified from the change property curve of a power-source current which changes according to change of supply voltage where the logic actuation test pattern which abnormalities generate is impressed, in a supply voltage pair power-source current characteristic, a power-source current is characterized by detecting failure mode, using respectively the inclination of the supply voltage value which begins to flow rapidly, and a power-source current, and the singular point of a property.
[0019]
[Function] If a CMOS logical circuit has a physical defect inside a circuit, outlying observation will appear in the quiescent-state power-source current called "Iddq (Quiesent Vdd Supply Current)" as a general tendency. This description is reference (M.). [Sanada "New] Application of Laser Beam to Failure analysis of LSI with Multi-metal layers" MicroElectronics and Reliability, Vol.33, No.7, and pp.993- 1009 and 1993 -- M.Sanada "Evaluation and Detection ofCMOS-LSI with Abnormal Iddq" MicroElectronics and Reliability, Vol.35, No.3, and pp.619- it is clear at 629 and 1995.
[0020] This invention uses the abnormal occurrence condition of this Iddq value. That is, it is characterized by to specify failure mode by inputting into an input terminal FTP which the abnormalities in Iddq which flow exceeding a predetermined value generate, and investigating the relation of the power-source current which changes when changing the supply voltage called the "V-I property" then acquired, when the logic actuation test pattern called "FTP (Function Test Pattern)" is inputted into the input terminal of a CMOS logical circuit. The test pattern which the abnormalities in Iddq which actualize the physical failure inside a circuit generate is inputted into an input terminal. Moreover it can specify failure mode from the curve of the V-I property then acquired, in this invention Where fixed supply voltage is impressed as an approach of changing the power-source impression environment of LSI to measure, every time amount of arbitration The configuration of a property where it changed by measuring the V-I property in FTP in the abnormalities in Iddq which flow exceeding a predetermined value, The configuration of a property where it changed by measuring the above-mentioned V-I property for every time amount of arbitration where fixed Iddq abnormal current is passed, Since the V-I property detected by making the configuration of the V-I property of changing by impressing a pulse voltage, and the polarity of supply voltage to impress into reverse was used so that it might superimpose on the supply voltage currently impressed, Failure mode can be specified where the curve of a V-I property is emphasized.
[0021] Moreover, by changing the outside temperature of LSI as an approach of changing the physical environment of LSI to measure in this invention Since change of the V-I property before and behind a temperature change was inspected or change of the V-I property of changing with the existence of an exposure of the light on the front face of a chip of LSI, the existence of an exposure of an electron beam, and the existence of an exposure of ion was inspected, Failure mode can be specified where the curve of a V-I property is emphasized.
[0022] Furthermore, this invention is characterized by specifying failure mode from change of the V-I property of changing by performing the device of power-source impression and the combination of the physical environment of LSI which were mentioned above, in order to detect the singularity of a V-I property.
[0023] The parameter used since failure mode is specified in the V-I property mentioned above is the approach of specifying failure mode from the description of the configuration of the whole V-I property curve by this invention approach. Or the current on a V-I property curve is observing the parameter used in order to detect failure mode from the V-I property at the inclination (delta I/delta V value) of the electrical-potential-difference value which begins to flow rapidly, and a current, and the singular point (V, I value) of a V-I property.
[0024]
[Example] Next, the example of this invention is explained with reference to a drawing. Drawing 1 is the flow chart of one example of this invention approach, and is a flow chart which specifies the failure mode of the nonconformity generated inside the CMOS logical circuit. As shown in this drawing, FTP when the abnormalities in Iddq which first measure leakage current (static power-source current) Iddq in the quiescent state of logic actuation when inputting two or more known logic actuation test patterns (FTP) one by one from the input terminal of a CMOS logical circuit, respectively, among those flow exceeding a predetermined value occur is extracted (step 11).

[0025] Drawing 2 is a graph which shows FTP at this time, and the relation of an Iddq value, a x axis shows the number of FTP and the y-axis shows an Iddq value. In this graph, the abnormalities in Iddq have occurred in FTP (P1) and (P2). Specification of failure mode uses this FTP (P1) and (P2).
[0026] Next, FTP extracted noting that the abnormalities in Iddq occurred in step 11 of drawing 1 is inputted into an input terminal, and the relation of the power-source current which changes when changing the supply voltage called the "V-I property" then acquired is investigated (step 12). Drawing 3 is a V-I property in FTP (P1) or FTP (P2) which has the abnormalities in an Iddq value detected from measurement of the FTP pair Iddq value in drawing 2 .
[0027] The power-source current of the CMOS logical circuit (large-scale integrated circuit: LSI) which a penetration current does not generate in a circuit in an all seems well has a physical defect in the interior of LSI to being below 1microA, and, generally the abnormalities in Iddq of hundreds to thousands times or more of a specification upper limit occur in the nonconformity article with which the defect affects a circuit (the above-mentioned reference reference).
[0028] Next, in step 12 of drawing 1 , the description of the investigated V-I property curve is extracted (step 13). however, failure mode should narrow down in a stationary environment -- when there is nothing, power-source impression of LSI is devised, or the physical environment of LSI to measure is changed, and failure mode is clearly actualized by emphasizing the description of a V-I property curve (step 14).
[0029] As the above-mentioned environmental acceleration approach, as a former device of power-source impression ** By measuring the V-I property for every time amount of arbitration, where fixed supply voltage is impressed By measuring the V-I property for every time amount of arbitration from the configuration of the property of changing, where the approach and the Iddq abnormal current of ** regularity which emphasize the description of a V-I property curve are passed How to emphasize the description of the V-I property curve when impressing a pulse voltage so that it may superimpose on the approach of emphasizing the description of a V-I property curve, and the supply voltage of which ** impression is done from the configuration of the property of changing, And there is a method of emphasizing the description of a V-I property curve by making into reverse the polarity of the supply voltage of which ** impression is done etc.
[0030] Moreover, there is a method of emphasizing the description of a V-I property curve among the approaches of changing the physical environment of the latter LSI, by the existence of an exposure of an electron beam on ** LSI chip front face which irradiates ion on change of an outside temperature of the **LSI whole [for example,], the existence of an exposure of the light to ** LSI chip front face, and ** LSI chip front face. Moreover, the description of a V-I property curve can also be emphasized with the combination of the physical environment of the irregular activity method of a power source, or LSI mentioned above.
[0031] And power-source impression of LSI is devised at step 14 in this way, or the physical environment of LSI to measure is changed, and after extracting the description of the V-I property extracted at step 13 based on fluctuation of the V-I property which was actualized clearly and investigated failure mode by emphasizing the description of a V-I property curve, failure mode is specified at step 15.
[0032] Next, the environmental acceleration approach of the above-mentioned step 14 is explained to a detail. First, there is a method which specifies failure mode from the configuration of a property where it changed, by measuring the V-I property for every time amount of arbitration where the fixed electrical potential difference of the aforementioned ** is impressed to LSI.
[0033] Drawing 4 is drawing showing change of the V-I property in the condition of having impressed the fixed electrical potential difference. Among drawing, a continuous line I is the V-I curve acquired when the abnormalities in Iddq were revealed, and a broken line II is the V-I curve in which the impedance decreased with time amount. This technique is effective in preventing that the reverse bias electric field more than pressure-proofing are built over a PN junction. Although the inclination for the singular point (for it to mention later) of a V-I property to change in this technique may be seen, that fluctuation is not directly related to failure mode.
[0034] This is explained with the representative circuit schematic of drawing 5 . This equal circuit is a circuit where the end of the parallel circuit of impedances Z1 and Z2 was connected to supply voltage Vdd, and the other end was connected to the gland through the component of an impedance Z, and shows the circuit which failure generated at the common node P of each component of impedances Z1, Z2, and Z. In this case, as for the leakage current path, the path which flows in order of Vdd->Z1 ->P->Z->GND shifts to a current path called Vdd->Z2 ->P->Z->GND to which the impedance decreased with the passage of time at the beginning.
[0035] Thus, since it changes in the direction where a leakage current path sets the failure generating part P as an origin or a core, and an impedance decreases, fluctuation is not directly related to failure mode. Therefore, by observing a changing point from fluctuation of a V-I property curve, the equal circuit which accelerated degradation of a failure part becomes clear, the leak in a failure part is emphasized, therefore specification of failure mode becomes easy.
[0036] Next, how to specify failure mode is explained from the configuration of a property where it changed, by measuring the V-I property for every time amount of arbitration, where the fixed Iddq abnormal current of the aforementioned ** is passed. Drawing 6 is drawing showing change of a V-I property where leakage current is kept constant. Among drawing, a continuous line III is the V-I curve acquired when the abnormalities in Iddq were revealed, and a broken line IV is the V-I curve in which the impedance decreased with time amount.
[0037] This technique is effective in order to prevent the open circuit by the electromigration especially generated with thin wiring, and induction of another failure mode by change of the upper layer by generation of heat by the high resistor by the increment in a current. The same inclination as **** also actualizes this technique, and the leak in a failure part is emphasized, therefore specification of failure mode becomes easy.
[0038] Next, the method which sees fluctuation of a V-I property is explained, superimposing a pulse voltage on supply voltage as a method which devises the supply voltage of LSI of the aforementioned **. Drawing 7 shows system configuration drawing in this case. In this drawing, the constant voltage and test pattern (FTP) which were generated by the constant voltage power supply and the test pattern generator 21 are supplied to LSI23 carried on the board 22. Moreover, the voltmeter 24 and ammeter 25 for measuring a V-I property are installed during GND wiring connected to the GND terminal of between each Vdd and GND terminal and LSI23, and the signal is connected to the personal computer (it abbreviates to a personal computer hereafter) 27, or the curve tracer 28 through the cable 26. Furthermore, the source 29 of a pulse voltage is installed on the path between a constant voltage power supply 21 and a board 22, and the supply voltage which superimposed the pulse voltage is impressed to LSI23.

[0039] The amplitude of the output pulse electrical potential difference of the source 29 of a pulse voltage is held down to less than [0.5V]. This reason is for preventing that forward bias of the PN junction is carried out, and a current begins to flow. The electrical potential differences which generally begin to flow by forward bias are only Abbreviation 0.65V-0.7V, and it is led from a degree type.
[0040] V** (kT/q), In (Is/I) However, it is referred to as I=1microA.
[0041] (k: A Boltzmann's constant, T:absolute temperature, the amount of q:electronic charge, Is:saturation current value)

This technique can distinguish whether it is placed between the paths which the penetration current has generated by the PN junction.
[0042] Drawing 8 is drawing explaining an example of the revealed failure mode, when a pulse voltage is superimposed on supply voltage. The V-I property that the continuous line V is not superimposed on the pulse voltage, and VI are the V-I properties of being superimposed on the pulse voltage, among this drawing. The difference in the property of V and VI is that the peak (inside a and b of drawing) has occurred in about 0.2 V and 1.8V in the property VI. This phenomenon shows that the PN junction is the forward direction one step at a time by a points and b points.
[0043] A physical defect exists in a semi-conductor substrate, or that a PN junction intervenes on the path of a penetration current can consider the short circuit of wiring by dielectric breakdown, and the inside of a well (Well).
[0044] Drawing 9 is an example of the V-I property when making the polarity of applied voltage into reverse, among this drawing, a continuous line VII is the V-I reverse property of normal LSI, and a broken line VIII is the V-I reverse property of LSI of having a physical defect in an internal circuitry. This kind of curve VIII is short between power sources, it is the mode of PN-junction destruction and a certain amount of failure mode is specified by this test again.
[0045] Next, how to emphasize the description of a V-I property curve because the outside temperature of the whole LSI of ** makes it change as an approach of changing the physical environment of said LSI is explained. Drawing 10 puts LSI into a thermostat, where FTP which the abnormalities in Iddq generate is inputted, and it shows system configuration drawing which looks at fluctuation of a V-I property, carrying out temperature acceleration.
[0046] In this drawing, the constant voltage and test pattern (FTP) which were generated by the constant voltage power supply and the test pattern generator 21 are supplied to LSI23 carried on the board 22. Moreover, the voltmeter 24 and ammeter 25 for measuring a V-I property are installed during GND wiring connected to the GND terminal of between each Vdd and GND terminal and LSI23, and the signal is connected to the personal computer 27 or the curve tracer 28 through the cable 26.
[0047] Furthermore, it is put into the LSI23 whole by the thermostat 30. This thermostat 30 is the structure which can carry out adjustable by a certain approach so that internal temperature may turn into desired temperature. Thus, change of the V-I property of the CMOS logical circuit of LSI23 when the temperature of the LSI23 whole changes is effective in detection of the leak which mainly originates in opening and the poor PN junction of a gate electrode. For example, opening of a gate electrode is explained with drawing 11 and drawing 12 .
[0048] Drawing 11 is an example of the revealed failure mode, when temperature acceleration of the whole LSI is carried out. Among this drawing, a continuous line IX is the case where temperature acceleration is not carried out, and a broken line X is a V-I property at the time of carrying out temperature acceleration. Being distinguished from the difference among properties IX and X is that the SURESSHORUDO electrical potential difference is related to channel resistance. That is, according to the temperature coefficient, it shifts in the direction where an impedance becomes large, and channel resistance is a SURESSHORUDO electrical potential difference further. It is decreasing according to the temperature characteristic (several mV/deg). This change appears notably, when one gate electrode of an inverter circuit is opened.
[0049] For example, drawing 12 is an example explaining an above-mentioned phenomenon, and is the inverter circuit which consisted of the P channel transistors (it is henceforth described as P-chTr) Q1 and the N channel transistors (it is henceforth described as N-chTr) Q2 of a couple. If the signal of high level (H) is impressed to an input when the gate electrode of P-chTrQ1 of an inverter circuit is opened (* in drawing shows), a penetration current will flow from Vdd to GND through N-chTrQ2 of an ON state through P-chTrQ1 of the Nor Marie ON state further.
[0050] If temperature acceleration of this inverter circuit is carried out, according to a temperature coefficient, the impedance shifts in the direction where it becomes large, and channel resistance of P-chTrQ1 of the Nor Marie ON state is the SURESSHORUDO electrical potential difference of N-chTrQ2 further. It decreases according to the temperature characteristic (several mV/deg), and change of the V-I property shown in drawing 11 actualizes.
[0051] Next, how to emphasize the description of a V-I property curve by the existence of the exposure of the light on the front face of an LSI chip of ** as an approach to which the physical environment of said LSI is changed is explained. Drawing 13 shows system configuration drawing of the system which inspects fluctuation of a V-I property by carrying out incidence of the light to the chip front face of LSI where FTP which the abnormalities in Iddq generate is inputted, or not carrying out incidence.
[0052] In this drawing, the constant voltage and test pattern (FTP) which were generated by the constant voltage power supply and the test pattern generator 21 are supplied to LSI23 carried on the board 22. Moreover, the voltmeter 24 and ammeter 25 for measuring a V-I property are installed during GND wiring connected to the GND terminal of between each Vdd and GND terminal and LSI23, and the signal is connected to the personal computer 27 or the curve tracer 28 through the cable 26.
[0053] Furthermore, the package was opened and the chip front face has exposed LSI23. The light source is installed above the chip side, and it does not irradiate on a chip front face at the light 31 from the light source. The characteristic thing in the existence of an exposure of light is changing leak substantially. Especially this phenomenon is seen by the defect resulting from a diffusion layer. For example, the V-I property currently observed since an electron is activated by the exposure of light in the PN-junction section moves in the direction in which an impedance decreases, and further, since the SURESSHORUDO electrical potential difference of a joint shifts in the reduction direction, existence of a joint is detected.
[0054] Next, how to emphasize the description of a V-I property curve by the existence of the exposure of the ion on the front face of an LSI chip of ** as an approach to which the physical environment of said LSI is changed is explained. Drawing 14 shows system configuration drawing of the system which inspects fluctuation of a V-I property by carrying out incidence of the ion to the chip front face of LSI where FTP which the abnormalities in Iddq generate is inputted, or

not carrying out incidence.
[0055] In this drawing, the constant voltage and test pattern (FTP) which were generated by the constant voltage power supply and the test pattern generator 21 are supplied to LSI23 carried on the board 22. Moreover, the voltmeter 24 and ammeter 25 for measuring a V-I property are installed during GND wiring connected to the GND terminal of between each Vdd and GND terminal and LSI23, and the signal is connected to the personal computer 27 or the curve tracer 28 through the cable 26.
[0056] Furthermore, since ion was irradiated, the package was opened, and the chip front face has exposed LSI23. The ion source 32 is installed above the chip side. Furthermore, the ion source 32 is installed into the vacuum lens-barrel 34 containing LS23 and a board 22.
[0057] The gate electrode of ion irradiation of a CMOS logical circuit is effective in the distinction in the defect who was opened. For example, when the condition that the gate electrode of P-chTrQ1 was opened in the inverter circuit shown in drawing 12 is considered, it will be in the operating state which "H" level inputted into the transistor when ion was accumulated in the gate electrode of P-chTrQ1 by ion irradiation, and since it shifts in the direction in which leak decreases, the gate electrode of P-chTrQ1 becomes detectable [the failure mode of having been open].
[0058] Next, how to emphasize the description of a V-I property curve by the existence of the exposure of the electron on the front face of an LSI chip of ** as an approach to which the physical environment of said LSI is changed is explained. Drawing 15 shows system configuration drawing of the system which inspects fluctuation of a V-I property by irradiating an electron or not irradiating the chip front face of LSI where FTP which the abnormalities in Iddq generate is inputted.
[0059] In this drawing, the constant voltage and test pattern (FTP) which were generated by the constant voltage power supply and the test pattern generator 21 are supplied to LSI23 carried on the board 22. Moreover, the voltmeter 24 and ammeter 25 for measuring a V-I property are installed during GND wiring connected to the GND terminal of between each Vdd and GND terminal and LSI23, and the signal is connected to the personal computer 27 or the curve tracer 28 through the cable 26.
[0060] Furthermore, since an electron was irradiated, the package was opened, and the chip front face has exposed LSI23. The electron gun 36 is installed above the chip side. Furthermore, the electron gun 36 is installed into the vacuum lens-barrel 37 containing LSI23 and a board 22.
[0061] Electron irradiation is also effective in the distinction in the defect to whom the gate electrode of a CMOS logical circuit was opened like ion irradiation. For example, when the condition that the gate electrode of P-chTrQ1 was opened in the inverter circuit shown in drawing 12 is considered, it will be in the operating state which "L" level inputted into the transistor when an electron was accumulated in the gate electrode of P-chTrQ1 by electron irradiation, and since leakage current shifts in the direction which increases further, the gate electrode of P-chTrQ1 becomes detectable [the failure mode of having been open].
[0062] On the contrary, in the condition that the gate electrode of N-chTrQ2 was opened, it will be in the operating state which "L" level inputted into the transistor when an electron was accumulated in the gate electrode of N-chTrQ2 by electron irradiation, and since it shifts in the direction in which leakage current decreases, it becomes detectable [the failure mode that the gate electrode of N-chTrQ2 was open].
[0063] CMOS which has a physical defect inside a circuit by changing an external environment as mentioned above By changing the V-I property of LSI, it becomes possible more to detect failure mode in a detail.
[0064] From the combination of change of the device of the applied voltage furthermore described above, and the external environment of LSI to CMOS It is possible to actualize the unique mode of the physical failure inside LSI.
[0065] The V-I property curve detected by the above actuation has two approaches which can perform detection of failure mode by holding the description. It is the approach which extracted the whole V-I property curve configuration and the singular point of a V-I property curve.
[0066] Drawing 16 is the whole V-I property curve configuration of explaining the first method. Since this draws a curve characteristic of each failure mode, the rough detection of it is attained.
[0067] Drawing 17 is another method and is a method which detects the singular point of a V-I property curve, and the inclination of leak as a parameter. That is, those parameters are (Vb, Ib), (Vc, Ic) and the value (Vd, Id) which indicate the location (inside b, c, and d of drawing) of an electrical potential difference and a current where the inclination of a leakage current curve changes to be the electrical-potential-difference value (inside a of drawing) to which leakage current begins to flow, and the value (inside alpha, beta, and gamma of drawing) of each inclination. Here, the values alpha, beta, and gamma of each above-mentioned inclination are expressed with a degree type.
[0068] Alpha=Ib/(Vb-Va)
beta=(Ic-Ib)/(Vc-Vb)
gamma=(Id-Ic)/(Vd-Vc)
Since these parameters are quantifying and expressing the description of a V-I property, the equal circuit of a leak path can judge them clearly, therefore they can specify failure mode certainly.
[0069] When physical failure exists in the interior of a CMOS logical circuit as mentioned above, since the V-I property detected can acquire a unique property to each physical failure, it can detect failure mode from the judgment of the V-I property curve.
[0070] Next, how to specify failure mode from the description of the detected V-I property is described. Beforehand, correlation with the voltage-current property which originates in failure mode and its failure and is generated is collected as a database. There are two well-known methods in this. One is a method which computes the V-I property which sets failure as a fundamental logical circuit and is generated by circuit simulation. It opts for simulation based on an equal circuit from the device structure of LSI which builds in failure mode, it can compute the current value which flows an equal circuit top by fluctuating an electrical potential difference, and can output a V-I property. The 2nd is a method which collects the V-I properties which originate in failure mode and its failure and are generated from the failure analysis of broken LSI.
[0071] And the above-mentioned collected V-I properties are put in a database as the whole V-I property curve configuration mentioned above or singular point parameter value of a V-I property curve.
[0072] Next, failure mode is specified from the comparison of the similarity of the configuration of the detected V-I property, and the description of the V-I property in a database. The comparison technique is performed using a personal

computer or an engineering workstation.

TECHNICAL FIELD

[Industrial Application] This invention relates to the specific approach of failure mode, and when especially a certain logic test pattern is inputted, it relates to the approach of specifying the failure mode generated in the CMOS logical circuit which the abnormalities in leakage current in the quiescent state of the logic called Iddq generate.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Conventionally, the method of specifying the cause of generating of the failure generated inside the CMOS logical circuit from electrical characteristics was impossible except for the short circuit between power sources (short circuit between Vdd-GND). Therefore, the failure generating part was narrowed down using the logic test pattern, physical analysis of the failure part narrowed down to the degree was performed, and the cause of fault is investigated and detected.

[0003] First, narrowing down of a failure part had the typical technique of extracting the potential map of an irradiating point, and a logic wave by detecting the secondary electron which is called an EB tester and which irradiates an electron on wiring of a large-scale integrated circuit (LSI), and is generated.

[0004] Moreover, detection of a failure part had detected failure mode using microscopes (SEM, optical microscope, etc.) by performing appearance observation, or etching to a desired layer with laser etc. further, and observing [**** / exposing a failure part] by performing ******** of the part limited by the ion beam which is called FIB, and which converged.

[0005] The method using the emission microscope (EMS) as a method which presumes failure mode is learned conventionally, and it is proposed by the 4th time dependability symposium (Vol.13/No.3 / November, 1991) "examination of the failure analysis technique of LSI by luminescence wavelength distribution" P.71 to P.76 of REAJ. This method is an analysis method which presumes the failure mode of LSI by analyzing the spectrum of the light emitted from the failure part of LSI in an emission microscope.

[0006] Drawing 18 is an explanatory view for the analysis of LSI by the above-mentioned emission microscope. In this drawing, luminescence emitted from the failure part of LSI42 is observed by the optical microscope 43 placed above LSI42 carried on the DUT board 41. Luminescence observed by this optical microscope 43 is amplified with the font amplifier tube 45 called an image intensifier through the filter 44 which makes only the light wave length band of the arbitration called a band pass filter penetrate, is picturized by CCD camera 46, and is sent to an image processing system 47. In order that an emission microscope may detect minute luminescence from LSI42, a luminescence observation path is set in a dark room 48. Moreover, the image which was processed by the image processing system 47 and obtained is displayed by the cathode-ray tube (CRT) 49.

[0007] By this conventional failure mode specification approach, by combining the function which integrates the quantity of light detected in the emission microscope, and the filter 44 which makes only the light wave length band of arbitration penetrate with a band pass filter, the amount of luminescence for every wavelength band is measured, and failure mode is presumed by observing the spectrum resulting from each failure mode.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, according to this invention, the failure mode efficiently generated inside the CMOS logical circuit by un-destroying can be specified. That is, the test pattern which the abnormalities in Iddq which actualize the physical failure inside a circuit generate according to this invention is inputted into an input terminal, since failure mode can be specified from the curve of the V-I property then acquired, a failure generating part is narrowed down and the huge mandays and time amount for detecting failure mode further can be reduced.
[0076] Furthermore, since according to this invention failure mode can be specified where the curve of a V-I property is emphasized by performing the device of the power source for specifying much failure modes, or an external environment, the unique mode can be certainly presumed to each failure mode.
[0077] Furthermore, according to this invention, since it is displayed as a V-I property depending on the class of failure mode generated on the electrical circuit, the V-I property measured by the test pattern of the abnormalities in Iddq can specify failure mode easily by detecting the V-I property.

[Translation done.]

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[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] however, poor leak according [the failure mode from which the failure mode detected in an emission microscope is detected by the specific method of the conventional failure mode mentioned above in the band since the light wave length band of a band pass filter 44 is limited with 400 to 1000nm] to poor opening of the gate electrode on a CMOS logical circuit, and gate oxide destruction -- further -- high resistance -- it is the short circuit between wiring by the conductor etc., and the failure mode detected was limited.
[0009] Moreover, although the failure mode detected was plotted by the graph which took the amount of luminescence in an arbitration graduation scale to the Y-axis called "luminescence spectrum", and took wavelength to the X-axis, the luminescence spectrum of the failure mode mentioned above is [variation] and was not deterministic. For example, drawing 19 is luminescence spectrum which shows the relation of the amount of luminescence to each wavelength of poor opening (inside B of drawing) of gate oxide destruction (inside A of drawing), and a gate electrode. When the variation in the spectrum configuration is mostly considered for the same configuration, it becomes impossible for the amount of luminescence to each wavelength of poor opening of gate oxide destruction and a gate electrode to presume failure mode to accuracy so that drawing 19 may show.
[0010] Moreover, in order to have to perform failure analysis by the emission microscope from detection of a failure generating part first, it takes time amount great by specification (or presumption) of failure mode. Furthermore, the emission microscope had the fault of limiting the narrowing-down part of failure in order to make impossible detection of luminescence under wiring in LSI which has multilayer-interconnection structure. When leakage current was still larger, since the quantity of light became immense, it had a fault of it becoming impossible to use an emission microscope.
[0011] This invention was made in view of the above point, and aims at offering the specific approach of failure mode that failure mode can be easily specified by un-destroying by using the supply voltage pair power-source current characteristic in the test pattern which the abnormalities in leakage current in the quiescent state of the logic called Iddq generated.
[0012] Moreover, other objects of this invention are to offer the specific approach of failure mode that failure mode can be specified promptly.

[Translation done.]

MEANS

[Means for Solving the Problem] This invention inputs the logic actuation test pattern of arbitration one by one from the input terminal of a CMOS logical circuit in order to attain the above-mentioned object. The power-source current in the quiescent state of logic actuation of a CMOS logical circuit is measured, respectively. Among those, the logic actuation test pattern which the abnormalities to which the power-source current in the quiescent state of logic actuation flows exceeding a predetermined value generate is extracted. Failure mode is specified from the change property curve of a power-source current which changes according to change of supply voltage where the extracted logic actuation test pattern is impressed.

[0014] Moreover, the change property curve of a power-source current which changes according to change of supply voltage where the logic actuation test pattern which this invention extracted is impressed carries out the description of being the curve of a supply voltage pair power-source current characteristic which changes by changing the power-source impression environment of a CMOS logical circuit.

[0015] Where fixed supply voltage is impressed, change of the power-source impression environment of the above-mentioned CMOS logical circuit here The change for every time amount of the arbitration of a supply voltage pair current characteristic, Where a fixed abnormality quiescent-state power-source current is passed, or the change for every time amount of the arbitration of a supply voltage pair current characteristic, Or it is characterized by being impressing a pulse voltage to supply voltage and changing a supply voltage pair current characteristic, or making the polarity of supply voltage to impress into reverse, and changing a supply voltage pair current characteristic.

[0016] Moreover, the change property curve of a power-source current which changes according to change of supply voltage where the logic actuation test pattern which this invention extracted is impressed carries out the description of being the curve of a supply voltage pair power-source current characteristic which changes by changing the physical environment of a CMOS logical circuit.

[0017] Here, change of the physical environment of a CMOS logical circuit is characterized by being the existence of an exposure of the light on changing the outside temperature of a large-scale integrated circuit which has a CMOS logical circuit, or the front face of a chip of the large-scale integrated circuit which has a CMOS logical circuit, ion, or an electron.

[0018] Furthermore, in this invention, since failure mode is specified from the change property curve of a power-source current which changes according to change of supply voltage where the logic actuation test pattern which abnormalities generate is impressed, in a supply voltage pair power-source current characteristic, a power-source current is characterized by detecting failure mode, using respectively the inclination of the supply voltage value which begins to flow rapidly, and a power-source current, and the singular point of a property.

[Translation done.]

OPERATION

[Function] If a CMOS logical circuit has a physical defect inside a circuit, outlying observation will appear in the quiescent-state power-source current called "Iddq (Quiesent Vdd Supply Current)" as a general tendency. This description is reference (M. Sanada "New). Application of Laser Beam to Failure analysis of LSI with Multi-metal layers" MicroElectronics and Reliability, Vol.33, No.7, and pp.993- 1009 and 1993 -- M.Sanada "Evaluation and Detection ofCMOS-LSI with Abnormal Iddq" MicroElectronics and Reliability, Vol.35, No.3, and pp.619- it is clear at 629 and 1995.
[0020] This invention uses the abnormal occurrence condition of this Iddq value. That is, it is characterized by to specify failure mode by inputting into an input terminal FTP which the abnormalities in Iddq which flow exceeding a predetermined value generate, and investigating the relation of the power-source current which changes when changing the supply voltage called the "V-I property" then acquired, when the logic actuation test pattern called "FTP (Function Test Pattern)" is inputted into the input terminal of a CMOS logical circuit. The test pattern which the abnormalities in Iddq which actualize the physical failure inside a circuit generate is inputted into an input terminal. Moreover it can specify failure mode from the curve of the V-I property then acquired, in this invention Where fixed supply voltage is impressed as an approach of changing the power-source impression environment of LSI to measure, every time amount of arbitration The configuration of a property where it changed by measuring the V-I property in FTP in the abnormalities in Iddq which flow exceeding a predetermined value, The configuration of a property where it changed by measuring the above-mentioned V-I property for every time amount of arbitration where fixed Iddq abnormal current is passed, Since the V-I property detected by making the configuration of the V-I property of changing by impressing a pulse voltage, and the polarity of supply voltage to impress into reverse was used so that it might superimpose on the supply voltage currently impressed Failure mode can be specified where the curve of a V-I property is emphasized.
[0021] Moreover, the thing for which the outside temperature of LSI is changed as an approach of changing the physical environment of LSI to measure in this invention, Since change of the V-I property before and behind a temperature change was inspected or change of the V-I property of changing with the existence of an exposure of the light on the front face of a chip of LSI, the existence of an exposure of an electron beam, and the existence of an exposure of ion was inspected, failure mode can be specified where the curve of a V-I property is emphasized.
[0022] Furthermore, this invention is characterized by specifying failure mode from change of the V-I property of changing by performing the device of power-source impression and the combination of the physical environment of LSI which were mentioned above, in order to detect the singularity of a V-I property.
[0023] The parameter used since failure mode is specified in the V-I property mentioned above is the approach of specifying failure mode from the description of the configuration of the whole V-I property curve, by this invention approach. Or the current on a V-I property curve is observing the parameter used in order to detect failure mode from the V-I property at the inclination (delta I/delta V value) of the electrical-potential-difference value which begins to flow rapidly, and a current, and the singular point (V, I value) of a V-I property.

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS OPERATION EXAMPLE DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the flow chart of one example of this invention approach.
[Drawing 2] It is the graph which shows an example of the relation between FTP in the flow chart of drawing 1 , and an Iddq value.
[Drawing 3] It is an example of the supply voltage pair power-source current (V-I) property in FTP which has the abnormalities in an Iddq value detected from the graph of drawing 2 .
[Drawing 4] It is a V-I property in the condition of having impressed the fixed electrical potential difference.
[Drawing 5] It is the representative circuit schematic showing signs that the leak path changes in the direction where an impedance decreases by setting a failure generating part as an origin or a core.
[Drawing 6] It is drawing showing change of a V-I property where leakage current is kept constant.
[Drawing 7] It is system configuration drawing of an example when superimposing a pulse voltage on supply voltage.
[Drawing 8] It is drawing showing change of the V-I property when not superimposing on the time of superimposing a pulse voltage on supply voltage.
[Drawing 9] It is drawing showing an example of the V-I property when making the polarity of applied voltage into reverse.

[Drawing 10] It is the block diagram showing an example of the equipment which measures fluctuation of a V-I property, carrying out temperature acceleration.
[Drawing 11] It is drawing showing change of the V-I property when having not considered as the time of carrying out temperature acceleration of the whole LSI.
[Drawing 12] It is inverter circuit drawing explaining fluctuation of the V-I property by temperature acceleration.
[Drawing 13] It is the block diagram showing an example of equipment which inspects fluctuation of a V-I property by the existence of the incidence of light on an LSI chip front face.
[Drawing 14] It is the block diagram showing an example of equipment which inspects fluctuation of a V-I property by the existence of an exposure of ion on an LSI chip front face.
[Drawing 15] It is the block diagram showing an example of equipment which inspects fluctuation of a V-I property by the existence of an electronic exposure on an LSI chip front face.
[Drawing 16] It is the whole V-I property curve configuration of using in order to presume failure mode.
[Drawing 17] It is drawing showing an example of the singular point of the V-I property curve used as a parameter for presuming failure mode, and the inclination of leak.
[Drawing 18] It is an explanatory view for the analysis of LSI by the emission microscope.
[Drawing 19] It is the luminescence spectrum which shows the relation of the amount of luminescence to each wavelength of poor opening of gate oxide and a gate electrode.
[Description of Notations]
11-15 Each step of one example of this invention approach
21 Constant Voltage Power Supply and Test Pattern Generator
22 Board
23 Large-scale Integrated Circuit (LSI)
24 Voltmeter
25 Ammeter
26 Cable
27 Personal Computer (Personal Computer)
28 Curve Tracer
29 Source of Pulse Voltage
30 Thermostat
31 Light
32 Ion Source
34 37 Lens-barrel
36 Electron Gun

[Translation done.]

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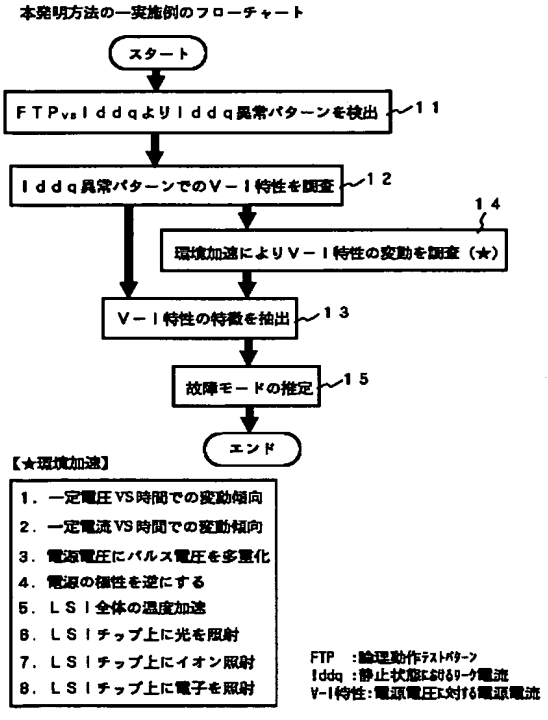
(54)【発明の名称】　故障モードの特定方法

(57)【要約】

【目的】　本発明は、非破壊で故障モードを容易に、しかも迅速に特定できる故障モードの特定方法を提供することを目的とする。

【構成】　ＣＭＯＳ論理回路にＦＴＰを入力したとき、論理動作の静止状態におけるリーク電流Ｉｄｄｑが、所定値を越えて流れるＩｄｄｑ異常が発生した時のＦＴＰを抽出する（ステップ１１）。Ｉｄｄｑ異常が発生したときのＦＴＰにおける”Ｖ－Ｉ特性”と称する電源電圧対電源電流の関係を調査する（ステップ１２）。次に、調査したＶ－Ｉ特性カーブの特徴を抽出する（ステップ１３）。定常環境にて故障モードが絞り込めないときは、ＬＳＩの電源印加を工夫したり、測定するＬＳＩの物理環境を変化させて、Ｖ－Ｉ特性カーブの特徴を強調することにより故障モードを明瞭に顕在化させる（ステップ１４）。次に、調査したＶ－Ｉ特性の変動に基づいて故障モードを特定する（ステップ１５）。



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【特許請求の範囲】

【請求項１】　ＣＭＯＳ論理回路の入力端子より任意の論理動作テストパターンを順次に入力して、該ＣＭＯＳ論理回路の論理動作の静止状態における電源電流をそれぞれ測定し、そのうち論理動作の静止状態における電源電流が所定値を越えて流れる異常が発生する論理動作テストパターンを抽出し、該抽出した論理動作テストパターンを印加した状態で電源電圧の変化に応じて変化する電源電流の変化特性カーブから故障モードを特定することを特徴とする故障モードの特定方法。

【請求項２】　前記抽出した論理動作テストパターンを印加した状態で電源電圧の変化に応じて変化する電源電流の変化特性カーブは、前記ＣＭＯＳ論理回路の電源印加環境を変化させることにより変化する電源電圧対電源電流特性のカーブであることを特徴する請求項１記載の故障モードの特定方法。

【請求項３】　前記ＣＭＯＳ論理回路の電源印加環境の変化は、一定電源電圧を印加した状態で前記電源電圧対電流特性の任意の時間毎の変化であることを特徴とする請求項２記載の故障モードの特定方法。

【請求項４】　前記ＣＭＯＳ論理回路の電源印加環境の変化は、一定の異常静止状態電源電流を流した状態で前記電源電圧対電流特性の任意の時間毎の変化であることを特徴とする請求項２記載の故障モードの特定方法。

【請求項５】　前記ＣＭＯＳ論理回路の電源印加環境の変化は、電源電圧にパルス電圧を印加して前記電源電圧対電流特性を変化させることであることを特徴とする請求項２記載の故障モードの特定方法。

【請求項６】　前記ＣＭＯＳ論理回路の電源印加環境の変化は、印加する電源電圧の極性を逆にして前記電源電圧対電流特性を変化させることであることを特徴とする請求項２記載の故障モードの特定方法。

【請求項７】　前記抽出した論理動作テストパターンを印加した状態で電源電圧の変化に応じて変化する電源電流の変化特性カーブは、前記ＣＭＯＳ論理回路の物理環境を変化させることにより変化する電源電圧対電源電流特性のカーブであることを特徴する請求項１記載の故障モードの特定方法。

【請求項８】　前記ＣＭＯＳ論理回路の物理環境の変化は、該ＣＭＯＳ論理回路を有する大規模集積回路の外部温度を変化させることであることを特徴とする請求項７記載の故障モードの特定方法。

【請求項９】　前記ＣＭＯＳ論理回路の物理環境の変化は、該ＣＭＯＳ論理回路を有する大規模集積回路のチップ表面への光の照射の有無であることを特徴とする請求項７記載の故障モードの特定方法。

【請求項１０】　前記ＣＭＯＳ論理回路の物理環境の変化は、該ＣＭＯＳ論理回路を有する大規模集積回路のチップ表面へのイオンの照射の有無であることを特徴とする請求項７記載の故障モードの特定方法。

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【請求項１１】　前記ＣＭＯＳ論理回路の物理環境の変化は、該ＣＭＯＳ論理回路を有する大規模集積回路のチップ表面への電子の照射の有無であることを特徴とする請求項７記載の故障モードの特定方法。

【請求項１２】　前記異常が発生する論理動作テストパターンを印加した状態で電源電圧の変化に応じて変化する電源電流の変化特性カーブから故障モードを特定するために、該電源電圧対電源電流特性において電源電流が急激に流れ始める電源電圧値、電源電流の勾配及び特性の特異点をそれぞれ用いて故障モードを検出することを特徴とする請求項１乃至１１のうちいずれか一項記載の故障モードの特定方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は故障モードの特定方法に係り、特にある論理テストパターンを入力したときにＩｄｄｑと称する論理の静止状態におけるリーク電流異常が発生するＣＭＯＳ論理回路に発生した故障モードを特定する方法に関する。

【０００２】

【従来の技術】従来、電気的特性からＣＭＯＳ論理回路の内部に発生した故障の発生原因を特定する方法は、電源間ショート（Ｖｄｄ－ＧＮＤ間のショート）を除いて不可能であった。そのため、論理テストパターンを用いて故障発生箇所の絞り込みを行い、次に絞り込んだ故障箇所の物理解析を行って故障原因を調査し、検出している。

【０００３】まず、故障箇所の絞り込みはＥＢテスターと称する、電子を大規模集積回路（ＬＳＩ）の配線上に照射し、発生する２次電子を検出することにより照射点の電位マップや論理波形を抽出する手法が代表的であった。

【０００４】また、故障箇所の検出は顕微鏡（ＳＥＭ、光学顕微鏡等）を用いて、外観観察を行ったり、さらにはレーザ等により所望の層までエッチングして故障箇所を露出させたり、ＦＩＢと称する集束したイオンビームにより限定された箇所の断面出しを行い、観察することにより故障モードを検出していた。

【０００５】故障モードを推定する方式としては従来、エミッション顕微鏡（ＥＭＳ）を用いた方式が知られており、ＲＥＡＪ第４回信頼性シンポジウム（Ｖｏｌ．１３／Ｎｏ．３／１９９１年１１月）Ｐ．７１～Ｐ．７６「発光波長分布によるＬＳＩの故障解析手法の検討」により提案されている。この方式はエミッション顕微鏡にてＬＳＩの故障箇所から発する光のスペクトラムを解析することによりＬＳＩの故障モードを推定する解析方式である。

【０００６】図１８は上記のエミッション顕微鏡によるＬＳＩの解析のための説明図である。同図において、ＤＵＴボード４１上に搭載されたＬＳＩ４２の上方に置か

れた光学顕微鏡４３により、ＬＳＩ４２の故障箇所から発する発光が観察される。この光学顕微鏡４３により観察された発光は、バンドパスフィルタと称する任意の光波長帯域だけを透過させるフィルタ４４を介してイメージインテンシファイアーと称するフォント増幅管４５にて増幅され、ＣＣＤカメラ４６により撮像されて画像処理装置４７に送られる。エミッション顕微鏡はＬＳＩ４２からの微小発光を検出するため、発光観察経路は暗室４８におかれる。また、画像処理装置４７により処理されて得られた画像は、陰極線管（ＣＲＴ）４９により表示される。

【０００７】この従来の故障モード特定方法では、エミッション顕微鏡にて検出した光量を積算する機能とバンドパスフィルタにより任意の光波長帯域だけを透過させるフィルタ４４を組み合わせることにより、各波長帯域毎の発光量を測定し、各故障モードに起因したスペクトルを観察することにより故障モードを推定する。

【０００８】

【発明が解決しようとする課題】しかるに、上述した従来の故障モードの特定方式では、エミッション顕微鏡にて検出される故障モードは、バンドパスフィルタ４４の光波長帯域が４００ｎｍから１０００ｎｍと限定されているため、その帯域で検出される故障モードはＣＭＯＳ論理回路上のゲート電極のオープン不良、ゲート酸化膜破壊によるリーク不良、さらには高抵抗導体による配線間ショート等であり、検出される故障モードが限定されていた。

【０００９】また、検出される故障モードは“発光スペクトラム”と称するＹ軸に任意目盛りスケールでの発光量、Ｘ軸に波長をとったグラフにプロットされるが、上述した故障モードの発光スペクトラムはバラツキがあり確定的ではなかった。例えば、図１９はゲート酸化膜破壊（図中Ａ）とゲート電極のオープン不良（図中Ｂ）の各波長に対する発光量の関係を示す発光スペクトラムである。図１９から分かるように、ゲート酸化膜破壊とゲート電極のオープン不良の各波長に対する発光量はほぼ同一形状のため、そのスペクトラム形状のバラツキを考えた時、正確に故障モードを推定することができなくなる。

【００１０】また、エミッション顕微鏡による故障解析はまず故障発生箇所の検出から行わねばならないため、故障モードの特定（あるいは推定）までに多大な時間がかかる。さらに、エミッション顕微鏡は多層配線構造を有するＬＳＩにおける配線下での発光の検出を不可能とするため、故障の絞り込み箇所を限定するという欠点があった。さらにリーク電流が大きいと光量は莫大となるため、エミッション顕微鏡を使用できなくなるという欠点があった。

【００１１】本発明は以上の点に鑑みなされたもので、Ｉｄｄｑと称する論理の静止状態におけるリーク電流異常が発生したテストパターンでの電源電圧対電源電流特性を用いることにより、非破壊で故障モードを容易に特定できる故障モードの特定方法を提供することを目的とする。

【００１２】また、本発明の他の目的は、故障モードの特定を迅速に行い得る故障モードの特定方法を提供することにある。

【００１３】

【課題を解決するための手段】本発明は上記の目的を達成するため、ＣＭＯＳ論理回路の入力端子より任意の論理動作テストパターンを順次に入力して、ＣＭＯＳ論理回路の論理動作の静止状態における電源電流をそれぞれ測定し、そのうち論理動作の静止状態における電源電流が所定値を越えて流れる異常が発生する論理動作テストパターンを抽出し、抽出した論理動作テストパターンを印加した状態で電源電圧の変化に応じて変化する電源電流の変化特性カーブから故障モードを特定するようにしたものである。

【００１４】また、本発明の抽出した論理動作テストパターンを印加した状態で電源電圧の変化に応じて変化する電源電流の変化特性カーブは、ＣＭＯＳ論理回路の電源印加環境を変化させることにより変化する電源電圧対電源電流特性のカーブであることを特徴する。

【００１５】ここで、上記のＣＭＯＳ論理回路の電源印加環境の変化は、一定電源電圧を印加した状態で電源電圧対電流特性の任意の時間毎の変化、あるいは、一定の異常静止状態電源電流を流した状態で電源電圧対電流特性の任意の時間毎の変化、あるいは、電源電圧にパルス電圧を印加して電源電圧対電流特性を変化させること、あるいは、印加する電源電圧の極性を逆にして電源電圧対電流特性を変化させることであることを特徴とする。

【００１６】また、本発明の抽出した論理動作テストパターンを印加した状態で電源電圧の変化に応じて変化する電源電流の変化特性カーブは、ＣＭＯＳ論理回路の物理環境を変化させることにより変化する電源電圧対電源電流特性のカーブであることを特徴する。

【００１７】ここで、ＣＭＯＳ論理回路の物理環境の変化は、ＣＭＯＳ論理回路を有する大規模集積回路の外部温度を変化させること、あるいは、ＣＭＯＳ論理回路を有する大規模集積回路のチップ表面への光あるいはイオンあるいは電子の照射の有無であることを特徴とする。

【００１８】更に、本発明では、異常が発生する論理動作テストパターンを印加した状態で電源電圧の変化に応じて変化する電源電流の変化特性カーブから故障モードを特定するために、電源電圧対電源電流特性において電源電流が急激に流れ始める電源電圧値、電源電流の勾配及び特性の特異点をそれぞれ用いて故障モードを検出することを特徴とする。

【００１９】

【作用】ＣＭＯＳ論理回路は回路内部に物理欠陥を有す

ると、一般的傾向として“Ｉｄｄｑ（Quiesent Vdd Supply Current）”と称する静止状態電源電流に異常値が現われる。この記述は文献(M.Sanada「New Application of Laser Beam to Failure analysis of LSI with Multi-metal layers」MicroElectronics and Reliability,Vol.33,No.7,pp.993～1009、1993やM.Sanada「Evaluation and Detection ofCMOS-LSI with Abnormal Iddq」MicroElectronics and Reliability,Vol.35,No.3,pp.619～629、1995)にて明らかである。

【００２０】本発明は、このＩｄｄｑ値の異常発生状態を利用したものである。すなわち、“ＦＴＰ（Function Test Pattern）”と称する論理動作テストパターンをＣＭＯＳ論理回路の入力端子に入力したとき、所定値を越えて流れるＩｄｄｑ異常が発生するＦＴＰを入力端子に入力し、その時得られる“Ｖ－Ｉ特性”と称する電源電圧を変化させた時変化する電源電流の関係を調査することにより、故障モードを特定することを特徴としている。回路内部の物理故障を顕在化させるＩｄｄｑ異常が発生するテストパターンを入力端子に入力し、その時得られるＶ－Ｉ特性のカーブより故障モードを特定化できる

また、本発明では、測定するＬＳＩの電源印加環境を変化させる方法として、一定の電源電圧を印加した状態で任意の時間毎の、所定値を越えて流れるＩｄｄｑ異常でのＦＴＰにおけるＶ－Ｉ特性を測定することで変化した特性の形状や、一定のＩｄｄｑ異常電流を流した状態で任意の時間毎の、上記Ｖ－Ｉ特性を測定することにより変化した特性の形状や、印加されている電源電圧に重畳するようにパルス電圧を印加することで変化するＶ－Ｉ特性の形状や、印加する電源電圧の極性を逆にすることで検出されるＶ－Ｉ特性を用いるようにしたため、Ｖ－Ｉ特性のカーブを強調した状態で故障モードを特定することができる。

【００２１】また、本発明では、測定するＬＳＩの物理環境を変化させる方法として、ＬＳＩの外部温度を変化させることにより、温度変化前後のＶ－Ｉ特性の変化を検査したり、ＬＳＩのチップ表面への光の照射の有無、電子ビームの照射の有無、そしてイオンの照射の有無により変化するＶ－Ｉ特性の変化を検査するようにしたため、Ｖ－Ｉ特性のカーブを強調した状態で故障モードを特定することができる。

【００２２】さらには、本発明は、Ｖ－Ｉ特性の特異性を検出するために、上述した電源印加の工夫やＬＳＩの物理環境の組合せを行うことにより変化するＶ－Ｉ特性の変化から故障モードを特定することを特徴としている。

【００２３】上述したＶ－Ｉ特性にて故障モードを特定するために用いるパラメータは、本発明方法では、Ｖ－Ｉ特性カーブの全体の形状の特徴から故障モードを特定する方法であり、または、そのＶ－Ｉ特性から故障モードを検出するために用いるパラメータは、Ｖ－Ｉ特性カーブ上の、電流が急激に流れはじめる電圧値、電流の勾配（ΔＩ／ΔＶ値）及び、Ｖ－Ｉ特性の特異点（Ｖ，Ｉ値）に注目している。

【００２４】

【実施例】次に、本発明の実施例について図面を参照して説明する。図１は本発明方法の一実施例のフローチャートで、ＣＭＯＳ論理回路の内部に発生した不具合の故障モードを特定するフローチャートである。同図に示すように、まず、ＣＭＯＳ論理回路の入力端子より既知の複数の論理動作テストパターン（ＦＴＰ）を順次に入力したときの、論理動作の静止状態におけるリーク電流（静的電源電流）Ｉｄｄｑをそれぞれ測定し、そのうち所定値を越えて流れるＩｄｄｑ異常が発生した時のＦＴＰを抽出する（ステップ１１）。

【００２５】図２はこの時のＦＴＰとＩｄｄｑ値の関係を示すグラフであり、ｘ軸はＦＴＰの番号を、ｙ軸はＩｄｄｑ値を示す。このグラフにおいて、ＦＴＰ（Ｐ１）、（Ｐ２）においてＩｄｄｑ異常が発生している。故障モードの特定は、このＦＴＰ（Ｐ１）、（Ｐ２）を用いる。

【００２６】次に、図１のステップ１１においてＩｄｄｑ異常が発生したとして抽出されたＦＴＰを入力端子に入力し、その時得られる”Ｖ－Ｉ特性”と称する電源電圧を変化させたとき変化する、電源電流の関係を調査する（ステップ１２）。図３は図２におけるＦＴＰ対Ｉｄｄｑ値の測定より検出したＩｄｄｑ値異常を有するＦＴＰ（Ｐ１）またはＦＴＰ（Ｐ２）でのＶ－Ｉ特性である。

【００２７】正常状態において回路に貫通電流が発生しないＣＭＯＳ論理回路（大規模集積回路：ＬＳＩ）の電源電流は１μＡ以下であるのに対して、ＬＳＩ内部に物理欠陥があり、その欠陥が回路に影響を与える不具合品においては、一般に規格上限値の数百倍から数千倍以上のＩｄｄｑ異常が発生する（前述の文献参考）。

【００２８】次に、図１のステップ１２において、調査したＶ－Ｉ特性カーブの特徴を抽出する（ステップ１３）。しかしながら、定常環境にて故障モードが絞り込めないときは、ＬＳＩの電源印加を工夫したり、測定するＬＳＩの物理環境を変化させて、Ｖ－Ｉ特性カーブの特徴を強調することにより故障モードを明瞭に顕在化させる（ステップ１４）。

【００２９】上記の環境加速方法として、前者の電源印加の工夫としては、①一定電源電圧を印加した状態で任意の時間毎のＶ－Ｉ特性を測定することにより、変化する特性の形状からＶ－Ｉ特性カーブの特徴を強調する方法、②一定のＩｄｄｑ異常電流を流した状態で任意の時間毎のＶ－Ｉ特性を測定することにより、変化する特性の形状からＶ－Ｉ特性カーブの特徴を強調する方法、③印加されている電源電圧に重畳するようにパルス電圧を

印加したときのＶ－Ｉ特性カーブの特徴を強調する方法、及び④印加する電源電圧の極性を逆にすることでＶ－Ｉ特性カーブの特徴を強調する方法などがある。

【００３０】また、後者のＬＳＩの物理環境を変化させる方法には、例えば⑤ＬＳＩ全体の外部温度の変化、⑥ＬＳＩチップ表面への光の照射の有無、⑦ＬＳＩチップ表面にイオンを照射する、⑧ＬＳＩチップ表面に電子ビームの照射の有無により、Ｖ－Ｉ特性カーブの特徴を強調する方法がある。また、上述した電源の変則的使用方式やＬＳＩの物理環境の組み合わせによりＶ－Ｉ特性カーブの特徴を強調することもできる。

【００３１】そして、このようにステップ１４でＬＳＩの電源印加を工夫したり、測定するＬＳＩの物理環境を変化させて、Ｖ－Ｉ特性カーブの特徴を強調することにより故障モードを明瞭に顕在化させて調査したＶ－Ｉ特性の変動に基づいて、ステップ１３で抽出したＶ－Ｉ特性の特徴を抽出した後、ステップ１５で故障モードを特定する。

【００３２】次に、上記のステップ１４の環境加速方法について詳細に説明する。まず、前記①の一定電圧をＬＳＩに印加した状態で任意の時間毎のＶ－Ｉ特性を測定することで、変化した特性の形状から故障モードを特定する方式がある。

【００３３】図４は一定電圧を印加した状態でのＶ－Ｉ特性の変化を示す図である。図中、実線ＩはＩｄｄｑ異常が発覚した時に取得したＶ－Ｉカーブであり、破線IIは時間とともにインピーダンスが減少していったＶ－Ｉカーブである。この手法はＰＮ接合に耐圧以上の逆バイアス電界がかかるのを防止するのに有効である。この手法においてＶ－Ｉ特性の特異点（後述する）が変化する傾向がみられることがあるが、その変動は故障モードに直接関係しない。

【００３４】このことについて、図５の等価回路図と共に説明する。この等価回路はインピーダンスＺ１とＺ２の並列回路の一端が電源電圧Ｖｄｄに接続され、他端がインピーダンスＺの素子を介してグランドに接続された回路で、インピーダンスＺ１、Ｚ２及びＺの各素子の共通接続点Ｐに故障が発生した回路を示す。この場合、リーク電流通路は、当初はＶｄｄ→Ｚ１→Ｐ→Ｚ→ＧＮＤの順で流れる通路が時間の経過と共にインピーダンスの減少したＶｄｄ→Ｚ２→Ｐ→Ｚ→ＧＮＤという電流通路へ移行していく。

【００３５】このように、リーク電流通路は故障発生箇所Ｐを起点若しくは中心としてインピーダンスの減少する方向へ変化していくから、変動は故障モードに直接関係しない。従って、Ｖ－Ｉ特性カーブの変動から変化点を注目することにより故障箇所の劣化を加速した等価回路が明確となり、そのため故障箇所におけるリークが強調され、従って、故障モードの特定が容易となる。

【００３６】次に、前記②の一定のＩｄｄｑ異常電流を流した状態で任意の時間毎のＶ－Ｉ特性を測定することで、変化した特性の形状から、故障モードを特定する方法について説明する。図６はリーク電流を一定に保った状態でＶ－Ｉ特性の変化を示す図である。図中、実線IIIはＩｄｄｑ異常が発覚した時に取得したＶ－Ｉカーブであり、破線IVは時間とともにインピーダンスが減少していったＶ－Ｉカーブである。

【００３７】この手法は電流の増加により、特に細い配線にて発生するエレクトロマイグレーションによる断線や、高抵抗体での発熱による上層の変化による別の故障モードの誘発を防止するために有効である。本手法も上述と同様な傾向が顕在化し、故障箇所におけるリークが強調され、従って、故障モードの特定が容易となる。

【００３８】次に、前記③のＬＳＩの電源電圧を工夫する方式として電源電圧にパルス電圧を重畳しながらＶ－Ｉ特性の変動をみる方式について説明する。図７はこの場合のシステム構成図を示す。同図において、定電圧電源及びテストパターン発生器２１により発生された定電圧及びテストパターン（ＦＴＰ）がボード２２上に搭載されているＬＳＩ２３に供給されている。また、Ｖ－Ｉ特性を測定するための電圧計２４及び電流計２５がそれぞれのＶｄｄとＧＮＤ端子間及びＬＳＩ２３のＧＮＤ端子へ接続されるＧＮＤ配線中に設置されており、その信号がケーブル２６を介してパーソナルコンピュータ（以下、パソコンと略す）２７やカーブトレーサ２８に接続されている。さらに定電圧電源２１とボード２２の間の通路上にパルス電圧源２９が設置されており、パルス電圧を重畳した電源電圧をＬＳＩ２３に印加している。

【００３９】パルス電圧源２９の出力パルス電圧の振幅は０．５Ｖ以下に抑えている。この理由はＰＮ接合が順バイアスされ、電流が流れはじめるのを防止するためである。一般に順バイアスにより流れ始める電圧は、約０．６５Ｖ～０．７Ｖぐらいであり、次式より導かれる。

【００４０】Ｖ≒（ｋＴ／ｑ）・ｌｎ（Ｉｓ／Ｉ）　但し、Ｉ＝１μＡとする。

【００４１】（ｋ：ボルツマン定数、Ｔ：絶対温度、ｑ：電子の電荷量、Ｉｓ：飽和電流値）

この手法は貫通電流が発生している通路にＰＮ接合が介在しているかを判別することが可能である。

【００４２】図８は電源電圧にパルス電圧を重畳した時、発覚する故障モードの一例を説明する図である。同図中、実線Ⅴはパルス電圧が重畳されていないＶ－Ｉ特性、VIはパルス電圧が重畳されているＶ－Ｉ特性である。ⅤとVIの特性の違いは、特性VIでは約０．２Ｖと１．８Ｖにピーク（図中ａ，ｂ）が発生していることである。この現象はａ点とｂ点でＰＮ接合が一段ずつ順方向になっていることを示すものである。

【００４３】貫通電流の通路上にＰＮ接合の介在することは、物理欠陥が半導体基板内に存在するか、または、

絶縁破壊による配線とウェル（Ｗｅｌｌ）内とのショートが考えられる。

【００４４】図９は印加電圧の極性を逆にした時のＶ－Ｉ特性の一例であり、同図中、実線VIIは正常ＬＳＩのＶ－Ｉ逆特性であり、破線VIIIは内部回路に物理的欠陥を有するＬＳＩのＶ－Ｉ逆特性である。この種のカーブVIIIは電源間ショートでありまた、ＰＮ接合破壊のモードであり、このテストによりある程度の故障モードが特定される。

【００４５】次に、前記ＬＳＩの物理環境を変化させる方法として⑤のＬＳＩ全体の外部温度の変化させることでＶ－Ｉ特性カーブの特徴を強調する方法について説明する。図１０はＩｄｄｑ異常が発生するＦＴＰを入力した状態でＬＳＩを恒温槽に入れ、温度加速をしながらＶ－Ｉ特性の変動を見るシステム構成図を示す。

【００４６】同図において、定電圧電源及びテストパターン発生器２１により発生された定電圧及びテストパターン（ＦＴＰ）がボード２２上に搭載されているＬＳＩ２３に供給されている。また、Ｖ－Ｉ特性を測定するための電圧計２４及び電流計２５がそれぞれのＶｄｄとＧＮＤ端子間及びＬＳＩ２３のＧＮＤ端子へ接続されるＧＮＤ配線中に設置されており、その信号がケーブル２６を介してパソコン２７やカーブトレーサ２８に接続されている。

【００４７】更に、ＬＳＩ２３全体は恒温槽３０に入れられている。この恒温槽３０は何らかの方法により、内部の温度が所望の温度となるように可変できる構造である。このようにしてＬＳＩ２３全体の温度が変化されたときの、ＬＳＩ２３のＣＭＯＳ論理回路のＶ－Ｉ特性の変化は、主にゲート電極のオープンやＰＮ接合不良に起因するリークの検出に有効である。例えばゲート電極のオープンに関して図１１及び図１２と共に説明する。

【００４８】図１１はＬＳＩ全体を温度加速した時、発覚する故障モードの一例である。同図中、実線IXは温度加速しない場合であり、破線Ｘは温度加速した場合のＶ－Ｉ特性である。特性IXとＸの違いから判別されることは、チャネル抵抗とスレッショールド電圧が関係していることである。すなわち、チャネル抵抗は温度係数に従って、インピーダンスが大きくなる方向へシフトしていき、さらにスレッショールド電圧は　温度特性（数ｍＶ／ｄｅｇ）に従って減少している。この変化はインバータ回路の一方のゲート電極がオープンになった時に顕著にあらわれる。

【００４９】例えば、図１２は上述の現象を説明する一例であり、一対のＰチャネルトランジスタ（以降、Ｐ－ｃｈＴｒと記す）Ｑ１とＮチャネルトランジスタ（以降、Ｎ－ｃｈＴｒと記す）Ｑ２にて構成されたインバータ回路である。インバータ回路のＰ－ｃｈＴｒＱ１のゲート電極がオープンとなった時（図中★で示す）、入力にハイレベル（Ｈ）の信号が印加されると、Ｖｄｄからノーマリーオン状態のＰ－ｃｈＴｒＱ１を介し、更にオン状態のＮ－ｃｈＴｒＱ２を介してＧＮＤへ貫通電流が流れる。

【００５０】このインバータ回路が温度加速されるとノーマリーオン状態のＰ－ｃｈＴｒＱ１のチャネル抵抗は温度係数に従って、インピーダンスが大きくなる方向へシフトしていき、さらにＮ－ｃｈＴｒＱ２のスレッショールド電圧は　温度特性（数ｍＶ／ｄｅｇ）に従って減少し、図１１に示すＶ－Ｉ特性の変化が顕在化する。

【００５１】次に、前記ＬＳＩの物理環境を変化させる方法として⑥のＬＳＩチップ表面への光の照射の有無によりＶ－Ｉ特性カーブの特徴を強調する方法について説明する。図１３はＩｄｄｑ異常が発生するＦＴＰを入力した状態でＬＳＩのチップ表面に光を入射したり、入射しなかったりすることでＶ－Ｉ特性の変動を検査するシステムのシステム構成図を示す。

【００５２】同図において、定電圧電源及びテストパターン発生器２１により発生された定電圧及びテストパターン（ＦＴＰ）がボード２２上に搭載されているＬＳＩ２３に供給されている。また、Ｖ－Ｉ特性を測定するための電圧計２４及び電流計２５がそれぞれのＶｄｄとＧＮＤ端子間及びＬＳＩ２３のＧＮＤ端子へ接続されるＧＮＤ配線中に設置されており、その信号がケーブル２６を介してパソコン２７やカーブトレーサ２８に接続されている。

【００５３】更に、ＬＳＩ２３はパッケージが開封され、チップ表面が露出している。そのチップ面の上方に光源が設置され、光源からの光３１がチップ表面に照射されたりされなかったりする。光の照射の有無における特徴的なことはリークが大幅に変動することである。この現象は、特に拡散層に起因する欠陥にみられる。例えば、光の照射によりＰＮ接合部にて電子は活性化されるため、観察しているＶ－Ｉ特性はインピーダンスが減少する方向に動き、さらに、接合部のスレッショールド電圧は減少方向へ移行するため接合部の存在が検出される。

【００５４】次に、前記ＬＳＩの物理環境を変化させる方法として⑦のＬＳＩチップ表面へのイオンの照射の有無によりＶ－Ｉ特性カーブの特徴を強調する方法について説明する。図１４はＩｄｄｑ異常が発生するＦＴＰを入力した状態でＬＳＩのチップ表面にイオンを入射したり、入射しなかったりすることでＶ－Ｉ特性の変動を検査するシステムのシステム構成図を示す。

【００５５】同図において、定電圧電源及びテストパターン発生器２１により発生された定電圧及びテストパターン（ＦＴＰ）がボード２２上に搭載されているＬＳＩ２３に供給されている。また、Ｖ－Ｉ特性を測定するための電圧計２４及び電流計２５がそれぞれのＶｄｄとＧＮＤ端子間及びＬＳＩ２３のＧＮＤ端子へ接続されるＧＮＤ配線中に設置されており、その信号がケーブル２６

を介してパソコン２７やカーブトレーサ２８に接続されている。

【００５６】更に、ＬＳＩ２３はイオンを照射するためにパッケージが開封され、チップ表面が露出している。そのチップ面の上方にイオン源３２が設置されている。さらにそのイオン源３２はＬＳ２３及びボード２２を含む真空鏡筒３４中に設置されている。

【００５７】イオン照射はＣＭＯＳ論理回路のゲート電極がオープンになった不良において、その判別に有効である。例えば図１２に示したインバータ回路においてＰ－ｃｈＴｒＱ１のゲート電極がオープンになった状態を考えた時、イオン照射によりＰ－ｃｈＴｒＱ１のゲート電極にイオンが蓄積することによりそのトランジスタにあたかも”Ｈ”レベルが入力した動作状態となり、リークが減少する方向に移行するため、Ｐ－ｃｈＴｒＱ１のゲート電極がオープンであったという故障モードの検出が可能となる。

【００５８】次に、前記ＬＳＩの物理環境を変化させる方法として⑧のＬＳＩチップ表面への電子の照射の有無によりＶ－Ｉ特性カーブの特徴を強調する方法について説明する。図１５はＩｄｄｑ異常が発生するＦＴＰを入力した状態でＬＳＩのチップ表面に電子を照射したり、照射しなかったりすることでＶ－Ｉ特性の変動を検査するシステムのシステム構成図を示す。

【００５９】同図において、定電圧電源及びテストパターン発生器２１により発生された定電圧及びテストパターン（ＦＴＰ）がボード２２上に搭載されているＬＳＩ２３に供給されている。また、Ｖ－Ｉ特性を測定するための電圧計２４及び電流計２５がそれぞれのＶｄｄとＧＮＤ端子間及びＬＳＩ２３のＧＮＤ端子へ接続されるＧＮＤ配線中に設置されており、その信号がケーブル２６を介してパソコン２７やカーブトレーサ２８に接続されている。

【００６０】更に、ＬＳＩ２３は電子を照射するためにパッケージが開封され、チップ表面が露出している。そのチップ面の上方に電子銃３６が設置されている。さらにその電子銃３６はＬＳＩ２３及びボード２２を含む真空鏡筒３７中に設置されている。

【００６１】電子照射もまた、イオン照射と同様にＣＭＯＳ論理回路のゲート電極がオープンになった不良において、その判別に有効である。例えば図１２に示したインバータ回路においてＰ－ｃｈＴｒＱ１のゲート電極がオープンになった状態を考えた時、電子照射によりＰ－ｃｈＴｒＱ１のゲート電極に電子が蓄積することによりそのトランジスタにあたかも”Ｌ”レベルが入力した動作状態となり、リーク電流がさらに増大する方向に移行するため、Ｐ－ｃｈＴｒＱ１のゲート電極がオープンであったという故障モードの検出が可能となる。

【００６２】逆に、Ｎ－ｃｈＴｒＱ２のゲート電極がオープンになった状態の時は電子照射によりＮ－ｃｈＴｒＱ２のゲート電極に電子が蓄積することによりそのトランジスタにあたかも”Ｌ”レベルが入力した動作状態となり、リーク電流が減少する方向に移行するため、Ｎ－ｃｈＴｒＱ２のゲート電極がオープンであったという故障モードの検出が可能となる。

【００６３】以上のように外部環境を変化させることにより回路内部に物理的欠陥を有するＣＭＯＳ　ＬＳＩのＶ－Ｉ特性を変化させることにより、より詳細に故障モードを検出することが可能となる。

【００６４】さらに以上述べた印加電圧の工夫や、ＬＳＩの外部環境の変化の組合せからＣＭＯＳ　ＬＳＩ内部の物理故障の特異なモードを顕在化することが可能である。

【００６５】以上の操作により検出されるＶ－Ｉ特性カーブは、その特徴をつかむことにより故障モードの検出ができる、２つの方法がある。Ｖ－Ｉ特性カーブの全体形状とＶ－Ｉ特性カーブの特異点を抽出した方法である。

【００６６】図１６は第一の方式を説明するＶ－Ｉ特性カーブの全体形状である。これは各故障モードに特徴的なカーブを描くため、大まかな検出が可能となる。

【００６７】図１７はもう一つの方式であり、Ｖ－Ｉ特性カーブの特異点及びリークの勾配をパラメータとして検出する方式である。すなわち、それらのパラメータはリーク電流が流れはじめる電圧値（図中ａ）と、リーク電流カーブの勾配が変化する電圧、電流の位置（図中ｂ，ｃ，ｄ）を示す、（Ｖｂ，Ｉｂ），（Ｖｃ，Ｉｃ），（Ｖｄ，Ｉｄ）値と、各勾配の値（図中α、β、γ）である。ここで、上記の各勾配の値α、β、γは次式で表される。

【００６８】α＝Ｉｂ／（Ｖｂ－Ｖａ）

β＝（Ｉｃ－Ｉｂ）／（Ｖｃ－Ｖｂ）

γ＝（Ｉｄ－Ｉｃ）／（Ｖｄ－Ｖｃ）

これらのパラメータはＶ－Ｉ特性の特徴を定量化して表現しているため、リーク通路の等価回路が明確に判断でき、従って、確実に故障モードを特定化できる。

【００６９】以上のようにＣＭＯＳ論理回路の内部に物理故障が存在する時、検出されるＶ－Ｉ特性は各々の物理故障に対して特異な特性を得ることができるため、そのＶ－Ｉ特性カーブの判定から故障モードを検出できる。

【００７０】次に、検出したＶ－Ｉ特性の特徴から故障モードを特定化する方法を述べる。あらかじめ、故障モードとその故障に起因して発生する電圧－電流特性との相関をデータベースとして収集しておく。これには２つの公知の方式がある。１つは基本的な論理回路に故障を設定し、回路シミュレーションにより発生するＶ－Ｉ特性を算出する方式である。シミュレーションは、故障モードを内蔵するＬＳＩのデバイス構造より等価回路を基にして決定されるものであり、電圧を増減することで等

価回路上を流れる電流値を算出し、Ｖ－Ｉ特性を出力することができる。２つ目は故障したＬＳＩの故障解析から故障モードとその故障に起因して発生するＶ－Ｉ特性を収集する方式である。

【００７１】そして、収集した上記のＶ－Ｉ特性は上述したＶ－Ｉ特性カーブの全体形状やＶ－Ｉ特性カーブの特異点パラメータ値としてデータベース化される。

【００７２】次に、検出されたＶ－Ｉ特性の形状とデータベース内のＶ－Ｉ特性の特徴の類似性の比較から、故障モードを特定する。その比較手法はパソコンやエンジニアリングワークステーションを用いて行う。このようにして、本実施例によれば、非破壊にて、効率的にＣＭＯＳ論理回路内部に発生した故障モードを特定化できる。

【００７３】なお、本発明は上記の実施例に限定されるものではなく、例えば定常時のＩｄｄｑ値が小さな回路ならば、メモリ、アナログ回路さらにはマイクロコンピュータ等の回路にも利用できる。

【００７４】また、定常時に大きなＩｄｄｑ値が発生する回路において、定常時のＶ－Ｉ特性がわかれば、Ｉｄｄｑ異常が発生した時のＶ－Ｉ特性から定常時のＶ－Ｉ特性分を引算することにより、上記と同様、簡単に故障モードを特定できる。

【００７５】

【発明の効果】以上説明したように、本発明によれば、非破壊にて、効率的にＣＭＯＳ論理回路内部に発生した故障モードを特定化できる。すなわち、本発明によれば、回路内部の物理故障を顕在化させるＩｄｄｑ異常が発生するテストパターンを入力端子に入力し、その時得られるＶ－Ｉ特性のカーブより故障モードを特定化できるため、故障発生箇所を絞り込み、さらに故障モードを検出するための膨大な工数と時間を削減できる。

【００７６】さらに、本発明によれば、数々の故障モードを特定化するための電源や外部環境の工夫を行うことでＶ－Ｉ特性のカーブを強調した状態で故障モードを特定することができるため、各々の故障モードに特異なモードを確実に推定できる。

【００７７】さらに、本発明によれば、Ｉｄｄｑ異常のテストパターンにて測定したＶ－Ｉ特性は、電気回路上に発生した故障モードの種類に依存したＶ－Ｉ特性として表示されるため、そのＶ－Ｉ特性を検出することにより簡単に故障モードを特定できる。

【図面の簡単な説明】

【図１】本発明方法の一実施例のフローチャートである。

【図２】図１のフローチャートにおけるＦＴＰとＩｄｄｑ値の関係の一例を示すグラフである。

【図３】図２のグラフから検出したＩｄｄｑ値異常を有するＦＴＰでの電源電圧対電源電流（Ｖ－Ｉ）特性の一例である。

【図４】一定電圧を印加した状態でのＶ－Ｉ特性である。

【図５】故障発生箇所を起点若しくは中心としてインピーダンスの減少する方向へリーク通路が変化していく様子を示す等価回路図である。

【図６】リーク電流を一定に保った状態でＶ－Ｉ特性の変化を示す図である。

【図７】電源電圧にパルス電圧を重畳するときの一例のシステム構成図である。

【図８】電源電圧にパルス電圧を重畳したときと重畳していないときのＶ－Ｉ特性の変化を示す図である。

【図９】印加電圧の極性を逆にしたときのＶ－Ｉ特性の一例を示す図である。

【図１０】温度加速をしながらＶ－Ｉ特性の変動を測定する装置の一例を示す構成図である。

【図１１】ＬＳＩ全体を温度加速したときとしていないときのＶ－Ｉ特性の変化を示す図である。

【図１２】温度加速によるＶ－Ｉ特性の変動を説明するインバータ回路図である。

【図１３】ＬＳＩチップ表面に光の入射の有無によりＶ－Ｉ特性の変動を検査する装置の一例を示す構成図である。

【図１４】ＬＳＩチップ表面にイオンの照射の有無によりＶ－Ｉ特性の変動を検査する装置の一例を示す構成図である。

【図１５】ＬＳＩチップ表面に電子の照射の有無によりＶ－Ｉ特性の変動を検査する装置の一例を示す構成図である。

【図１６】故障モードを推定するために用いるＶ－Ｉ特性カーブの全体形状である。

【図１７】故障モードを推定するためのパラメータとして用いるＶ－Ｉ特性カーブの特異点及びリークの勾配の一例を示す図である。

【図１８】エミッション顕微鏡によるＬＳＩの解析のための説明図である。

【図１９】ゲート酸化膜とゲート電極のオープン不良の各波長に対する発光量の関係を示す発光スペクトラムである。

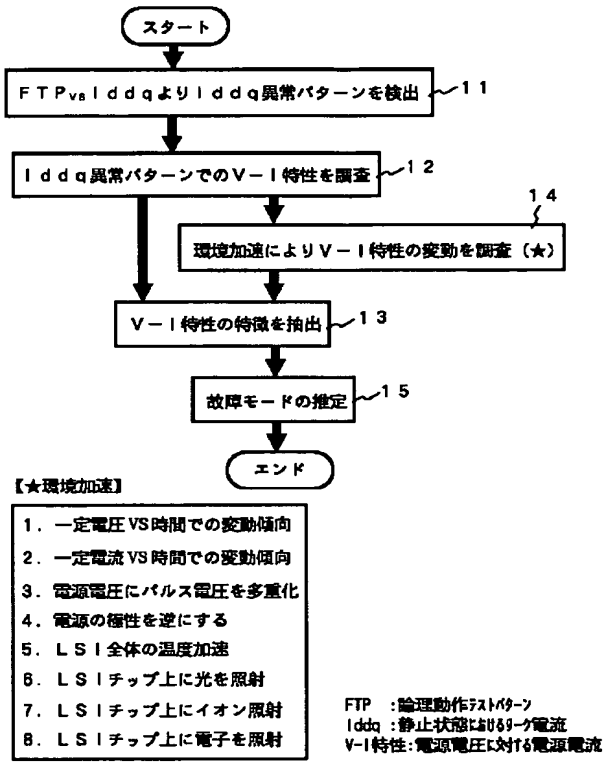
【符号の説明】

１１～１５　本発明方法の一実施例の各ステップ
２１　定電圧電源及びテストパターン発生器
２２　ボード
２３　大規模集積回路（ＬＳＩ）
２４　電圧計
２５　電流計
２６　ケーブル
２７　パーソナルコンピュータ（パソコン）
２８　カーブトレーサ
２９　パルス電圧源
３０　恒温槽

３１　光
３２　イオン源

【図１】

本発明方法の一実施例のフローチャート



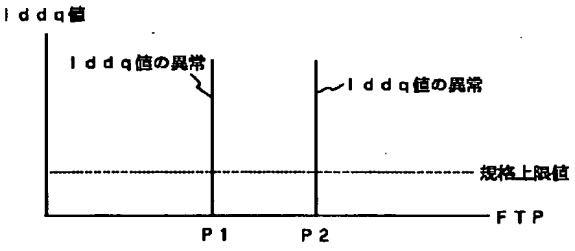
【図３】

図２のグラフから検出したＩｄｄｑ値以上を有するＦＴＰでの電源電圧対電源電流特性の一例

３４、３７　鏡筒
３６　電子銃

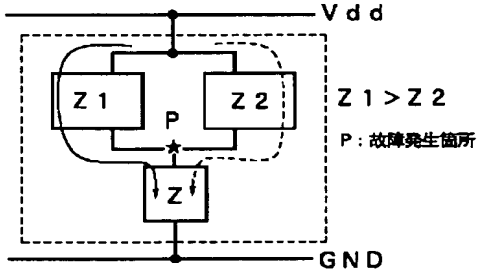
【図２】

図１のフローチャートにおけるFTPとIddq値の関係の一例を示すグラフ



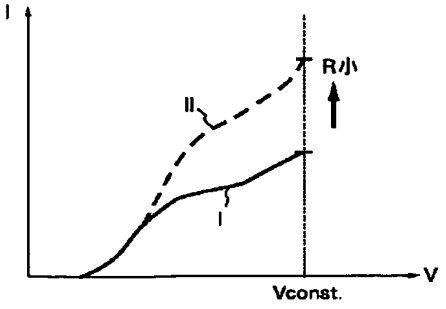
【図５】

リーク通路が変化していく様子を示す等価回路図



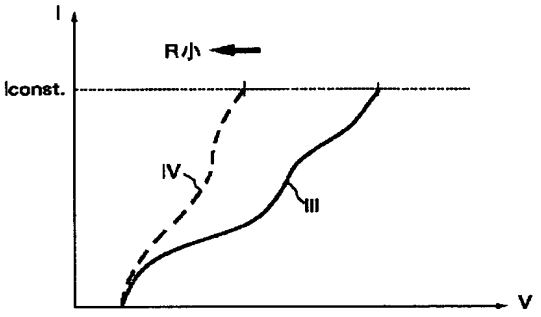
【図４】

一定電圧を印加した状態でのＶ－Ｉ特性



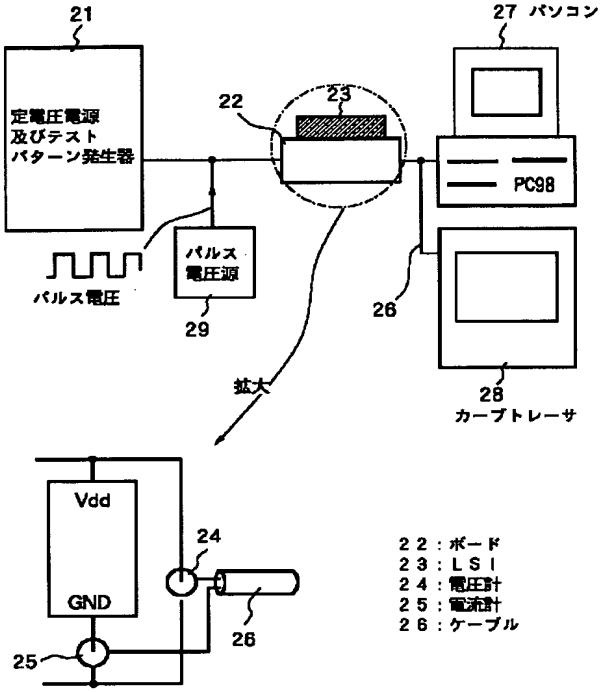
【図６】

リーク電流を一定に保った状態でＶ－Ｉ特性の変化を示す図



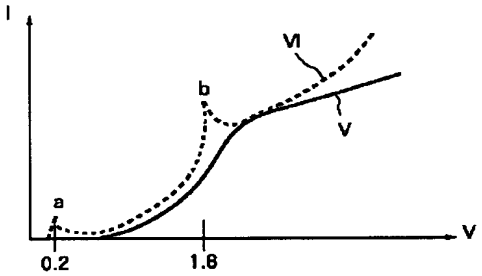
【図７】

電源電圧にパルス電圧を重畳するときの一例のシステム構成図



【図８】

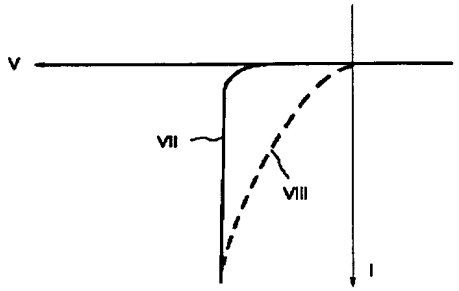
電源電圧にパルス電圧を重畳したときと重畳していないときとのＶ－Ｉ特性の変化を示す図



Ｖ：パルス電圧が重畳されていないＶ－Ｉ特性
ＶＩ：パルス電圧が重畳されているＶ－Ｉ特性

【図９】

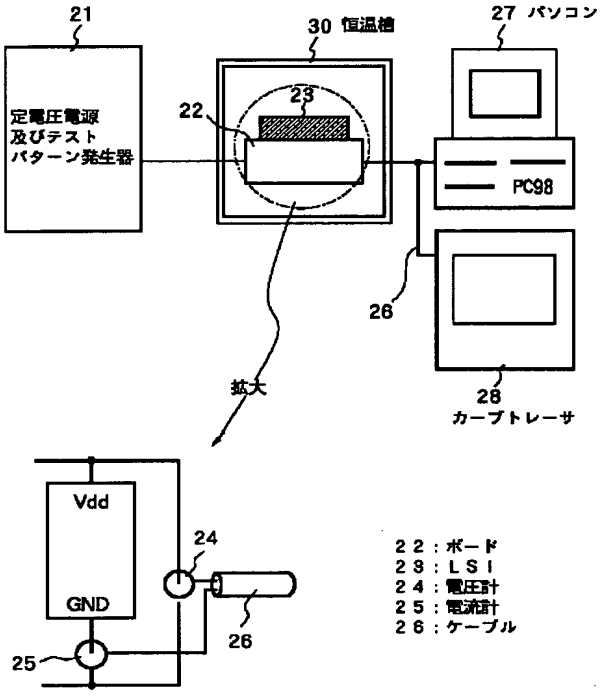
印加電圧の極性を逆にしたときのＶ－Ｉ特性の一例を示す図



ＶＩＩ：正常品のＶ－Ｉ逆特性
ＶＩＩＩ：内部回路に物理的欠陥を有するLSIのＶ－Ｉ逆特性

【図１０】

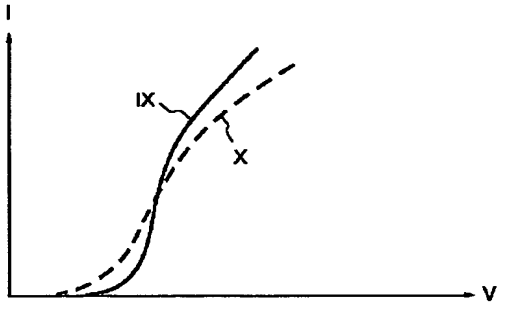
温度加速をしながらＶ－Ｉ特性の変動を測定する装置の一例の構成図



２２：ボード
２３：ＬＳＩ
２４：電圧計
２５：電流計
２６：ケーブル

【図１１】

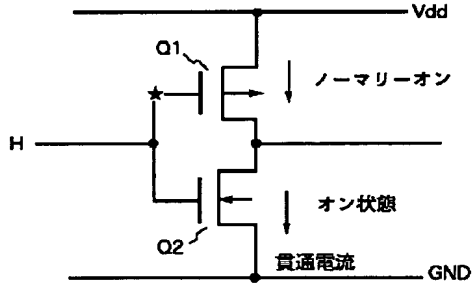
LSI全体を温度加速したときとしていないときのＶ－Ｉ特性の変化を示す図



IX：温度加速しない場合のＶ－Ｉ特性
X：温度加速した場合のＶ－Ｉ特性

【図１２】

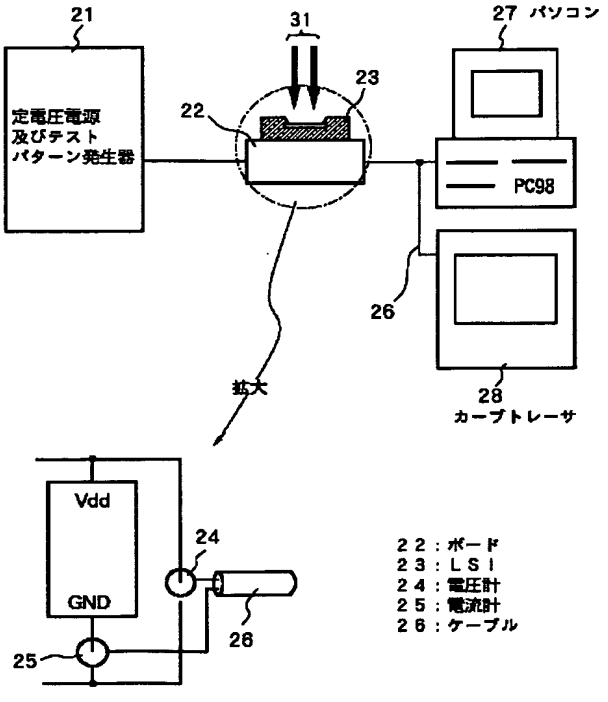
温度加速によるＶ－Ｉ特性の変動を説明するインバータ回路図



★：ゲート電極オープン

【図１３】

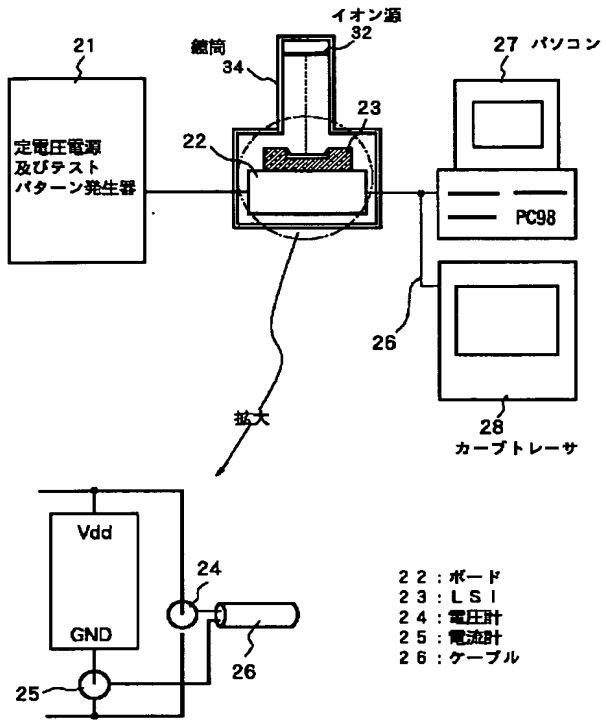
LSIチップ表面に光の入射の有無によりＶ－Ｉ特性の変動を検査する装置の一例の構成図



２２：ボード
２３：ＬＳＩ
２４：電圧計
２５：電流計
２６：ケーブル

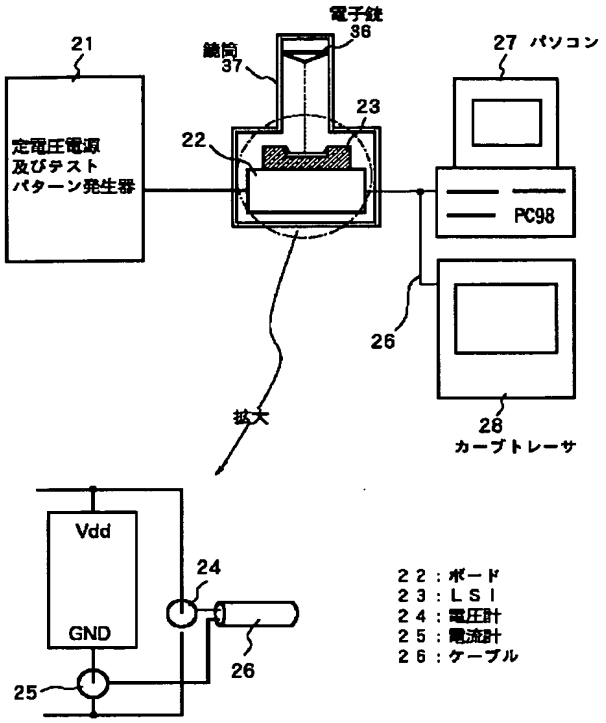
【図１４】

LSIチップ表面にイオンの入射の有無によりＶ－Ｉ特性の変動を検査する装置の一例の構成図



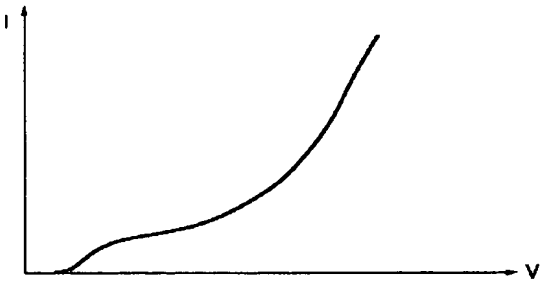
【図１５】

LSIチップ表面に電子の入射の有無によりＶ－Ｉ特性の変動を検査する装置の一例の構成図



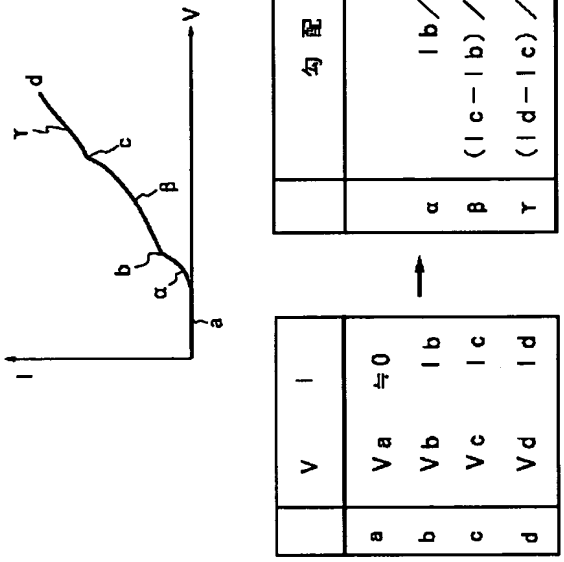
【図１６】

故障モードを推定するために用いるＶ－Ｉ特性カーブの全体形状



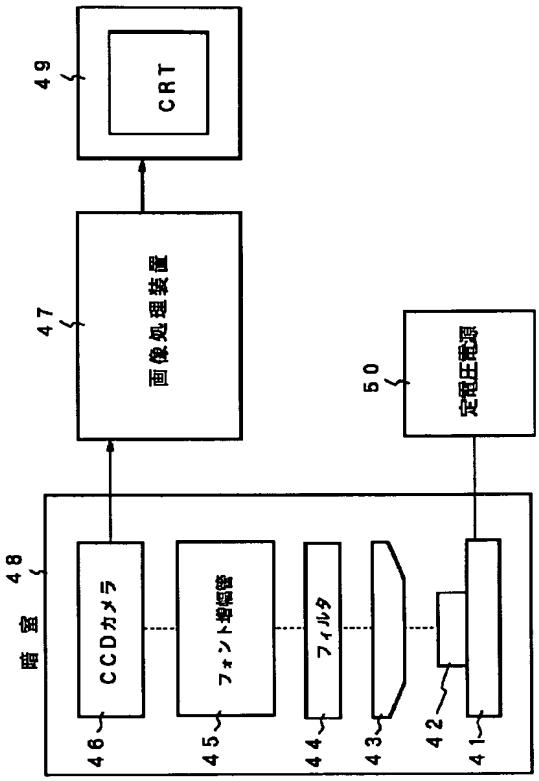
【図１７】

故障モードを推定するためのパラメータとして用いるＶ－Ｉ特性カーブの特異点及びリークの勾配の一例



【図１８】

エミッション顕微鏡によるＬＳＩの解析のための説明図



【図１９】

ゲート酸化膜とゲート電極のオープン不良の各波長に対する発光量の関係を示す発光スペクトラム